

1. Issue 7 Circuit Diagrams

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Figure 34	-	PCB layout, Bottom side/Bottom	2 of 2

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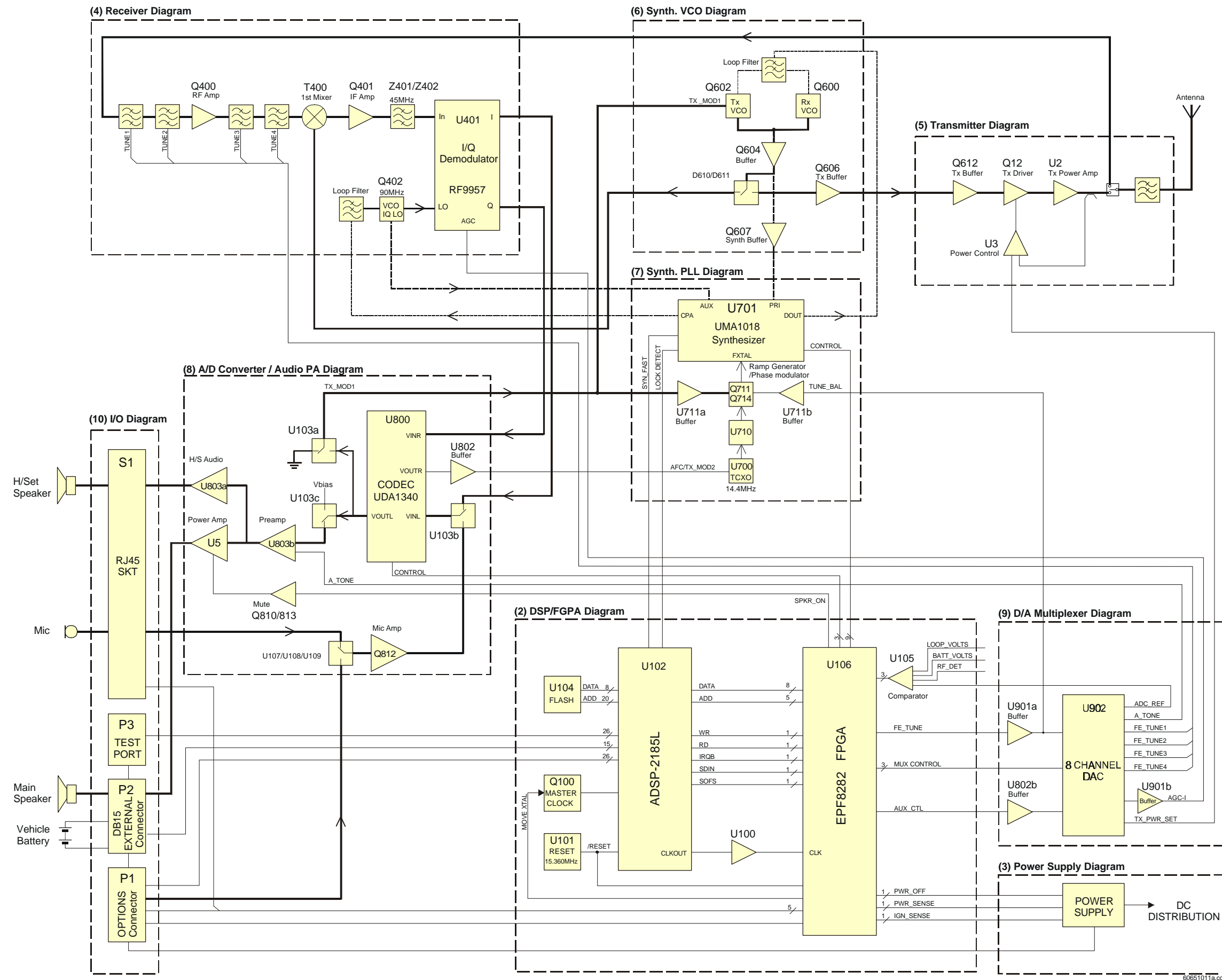


Figure 1 SRM9000 Block Diagram

Issue 7 Circuit Diagrams

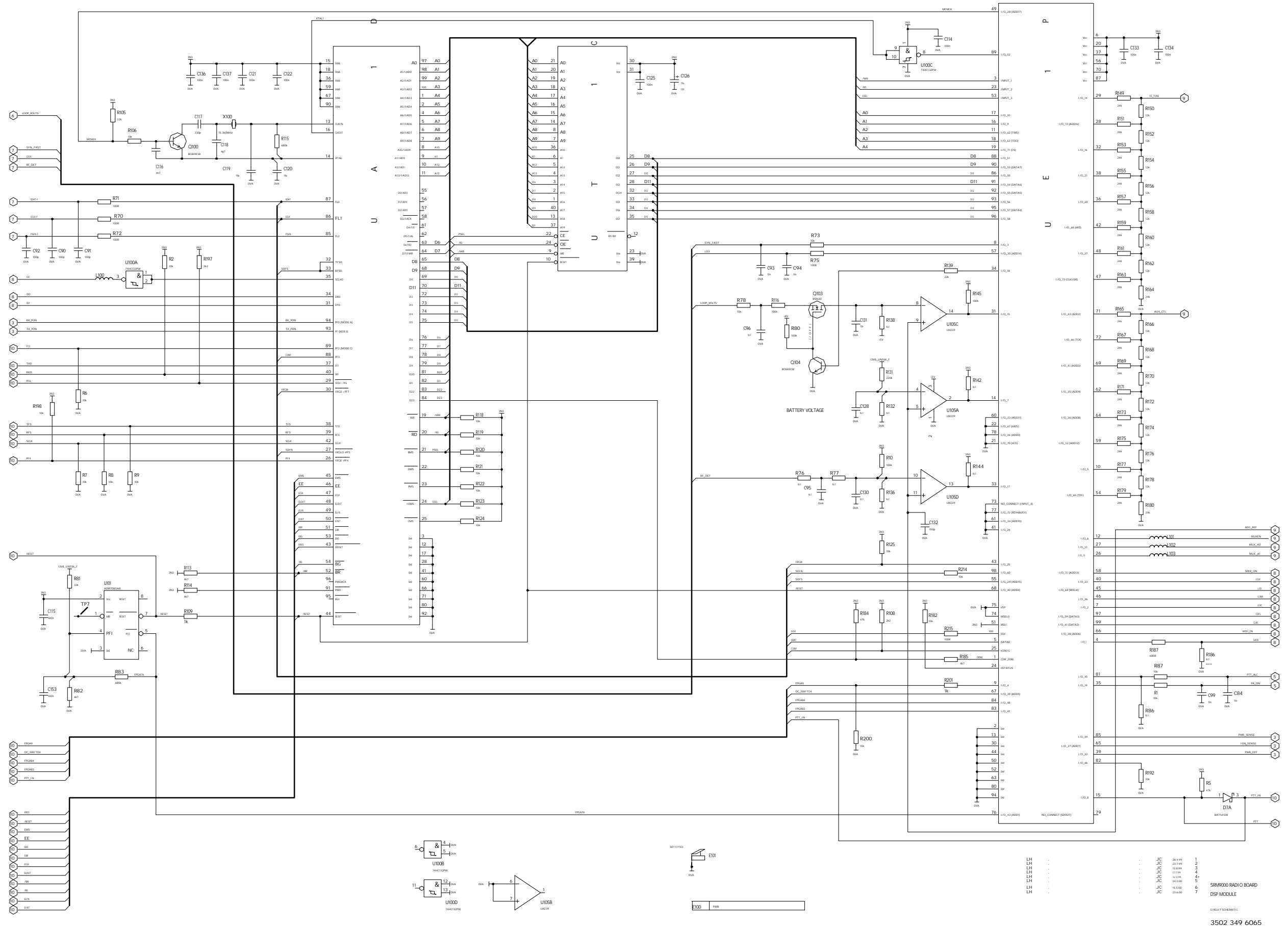
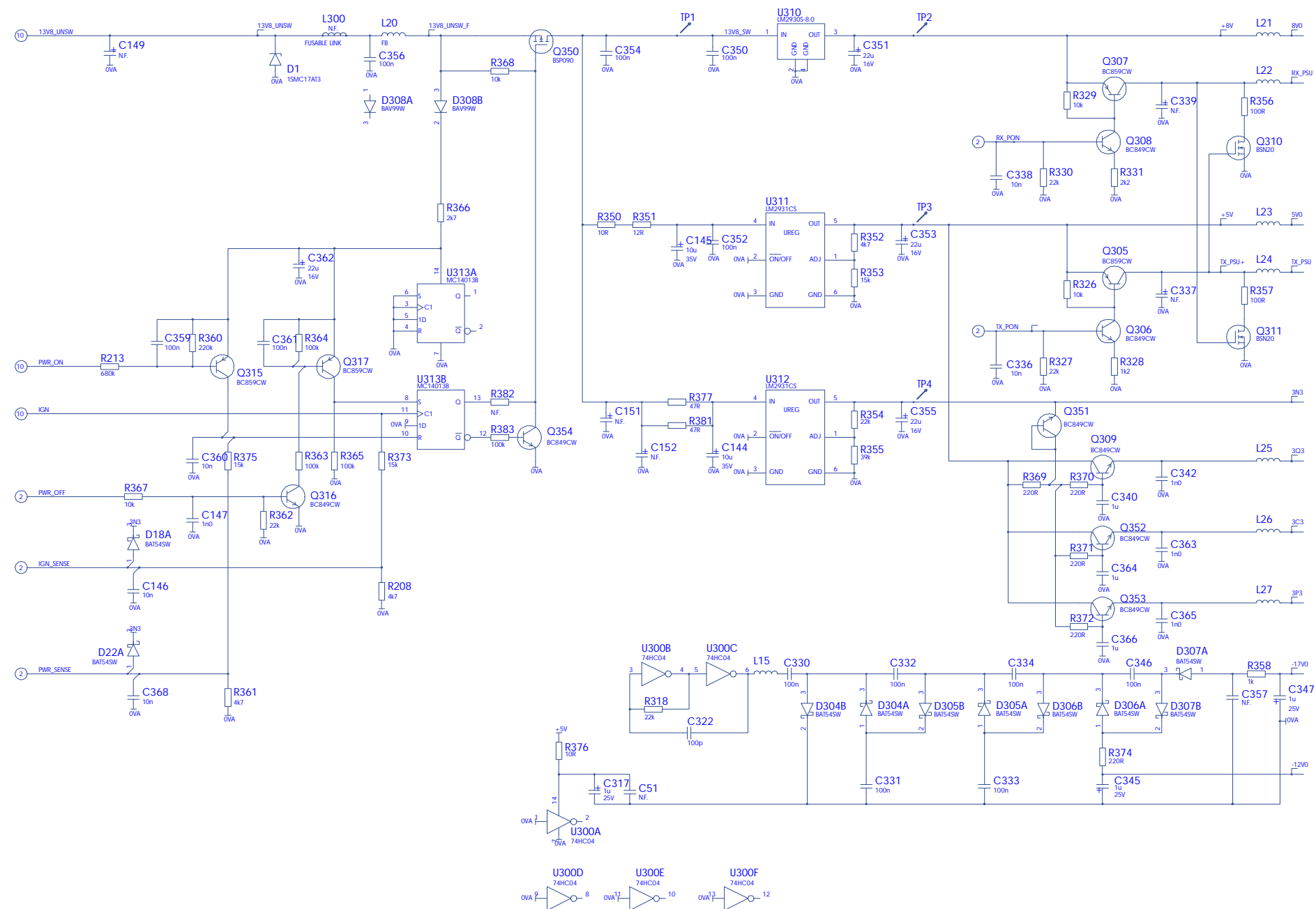


Figure 2 DSP and FGPA Schematic

Issue 7 Circuit Diagrams



ORDER	DRAWN	REMARKS	EXAM	APPRO	DATE	REV
LH	-	-	-	JC	15.9.99	1
LH	-	-	-	JC	17.11.99	2
LH	-	-	-	JC	13.6.99	3
LH	-	-	-	JC	17.11.99	4
LH	-	C359 CHANGE TO 100n	-	JC	16.12.99	5
LH	-	-	-	JC	17.11.99	6
LH	-	-	-	JC	24.2.00	5
LH	-	-	-	JC	15.6.00	6
LH	-	-	-	JC	23.6.00	7
LH	-	-	-	JC	17.7.00	7A

SMOOC PACIFIC MILGRAVE AUSTRALIA

RM9000 RADIO BOARD

PWY SUPPLY

CIRCUIT SCHEMATIC

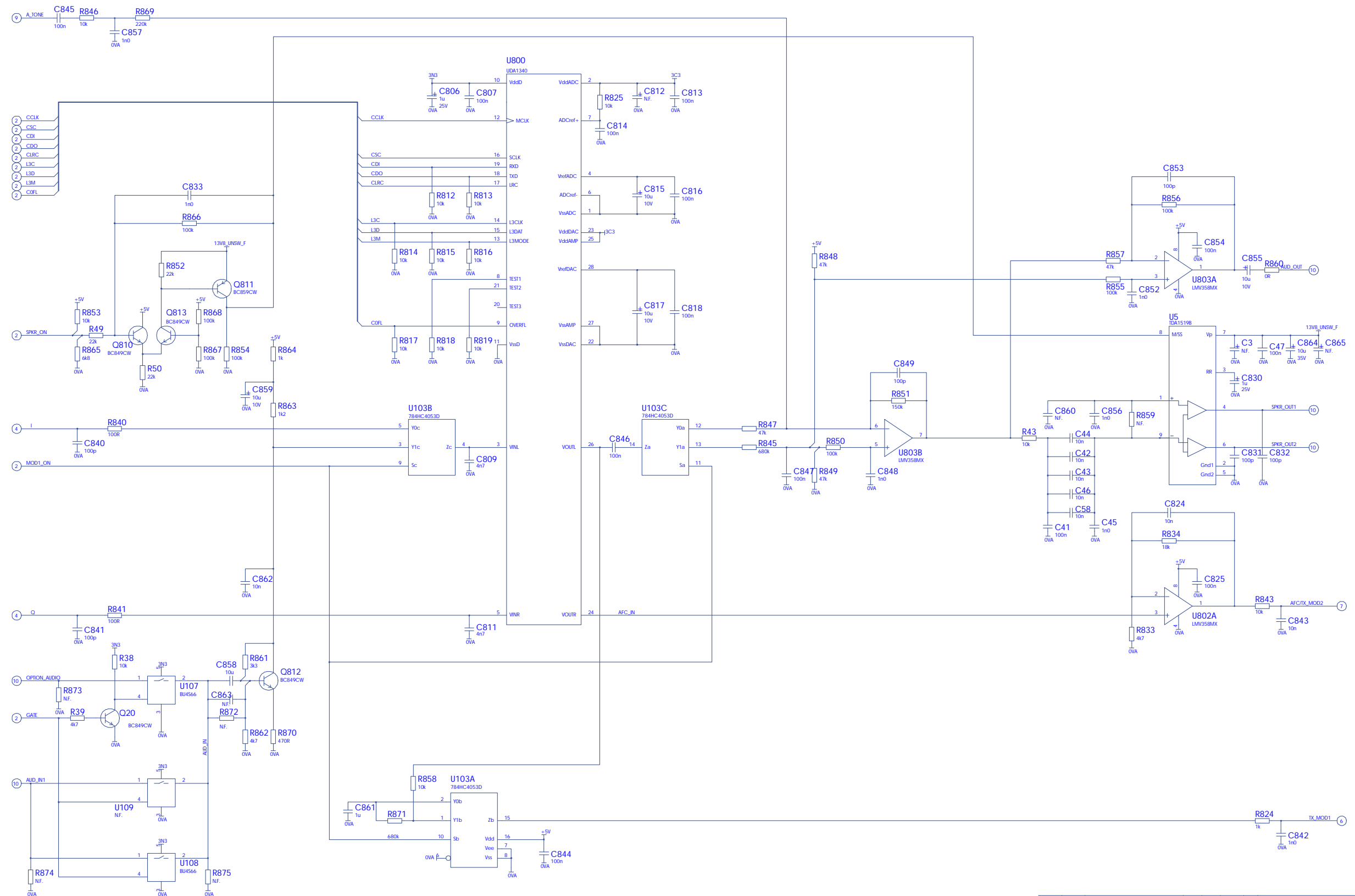
3502 349 6065

130 - 003

1/10

Figure 3 Power Supply Schematic

Issue 7 Circuit Diagrams



ORDER	DRAWN	REMARKS	EXAM	APPO	DATE	REV
LH	-	-	-	JC	28.4.99	1
LH	-	-	-	JC	7.7.99	2
LH	-	-	-	JC	13.8.99	3
LH	-	-	-	JC	17.11.99	4
LH	-	-	-	JC	24.2.00	5
LH	-	-	-	JC	16.5.00	6
LH	-	-	-	JC	23.9.00	7
LH	-	-	-	JC	17.7.00	7A

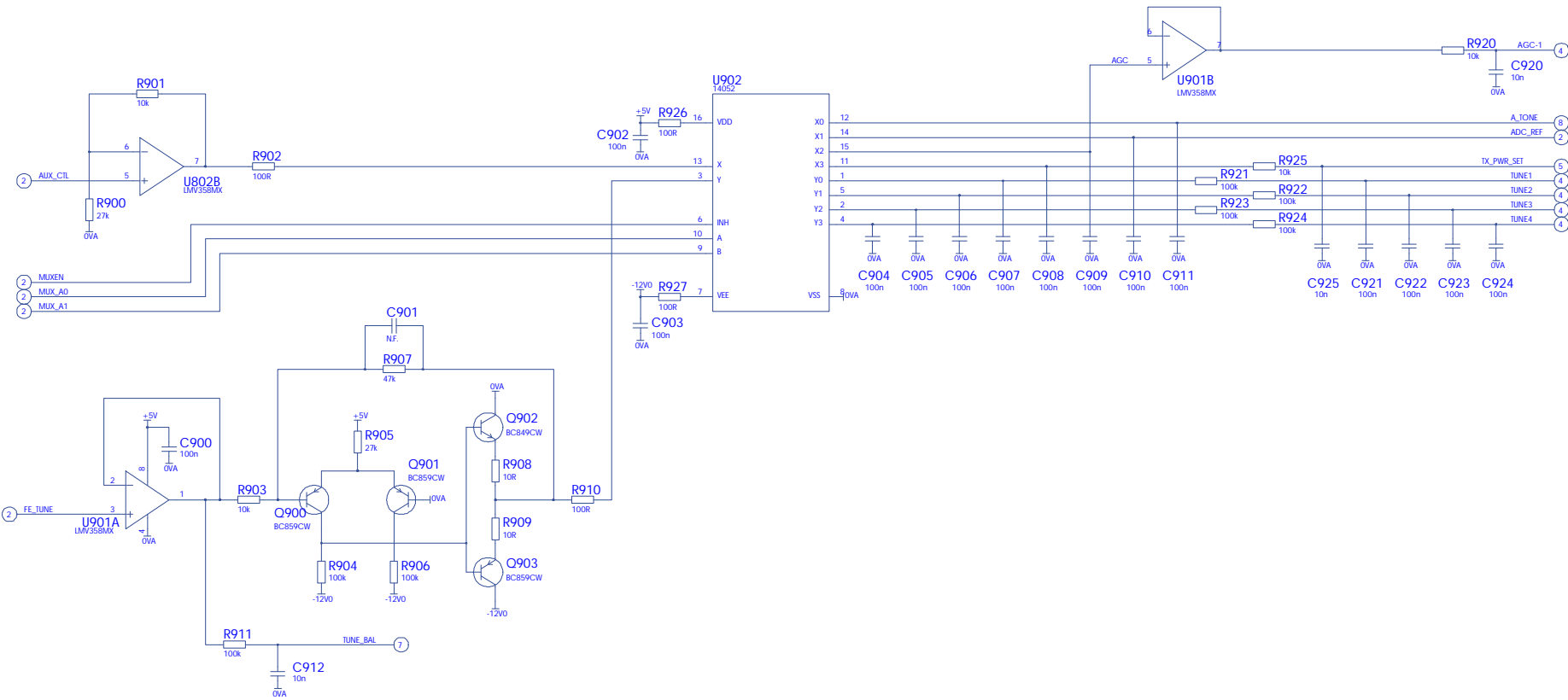
SIMOCO PACIFIC MULGRAVE AUSTRALIA

SRM9000 RADIO BOARD A/D CONVERTOR

CIRCUIT SCHEMATIC

130 - 008
010

Figure 4 A/D Converter Schematic



ORDER	DRAWN	REMARKS	EXAM	APPO	DATE	REV	SIMOCO PACIFIC MULGRAVE AUSTRALIA SRM9000 RADIO BOARD D/A CIRCUIT SCHEMATIC 3502 349 6065
LH	-	-	-	JC	28.4.99	1	
LH	-	-	-	JC	23.2.99	2	
LH	-	-	-	JC	13.6.99	3	
LH	-	-	-	JC	17.11.99	4	
LH	-	-	-	JC	16.12.99	4++	
LH	-	R900 CHANGED FROM 18K TO 27K	-	JC	25.1.00	5	
LH	-	-	-	JC	24.2.00	5	
LH	-	-	-	JC	15.5.00	6	
LH	-	-	-	JC	23.6.00	7	
LH	-	-	-	JC	17.7.00	7A	
130-009 010							

Figure 5 D/A Multiplexer Schematic

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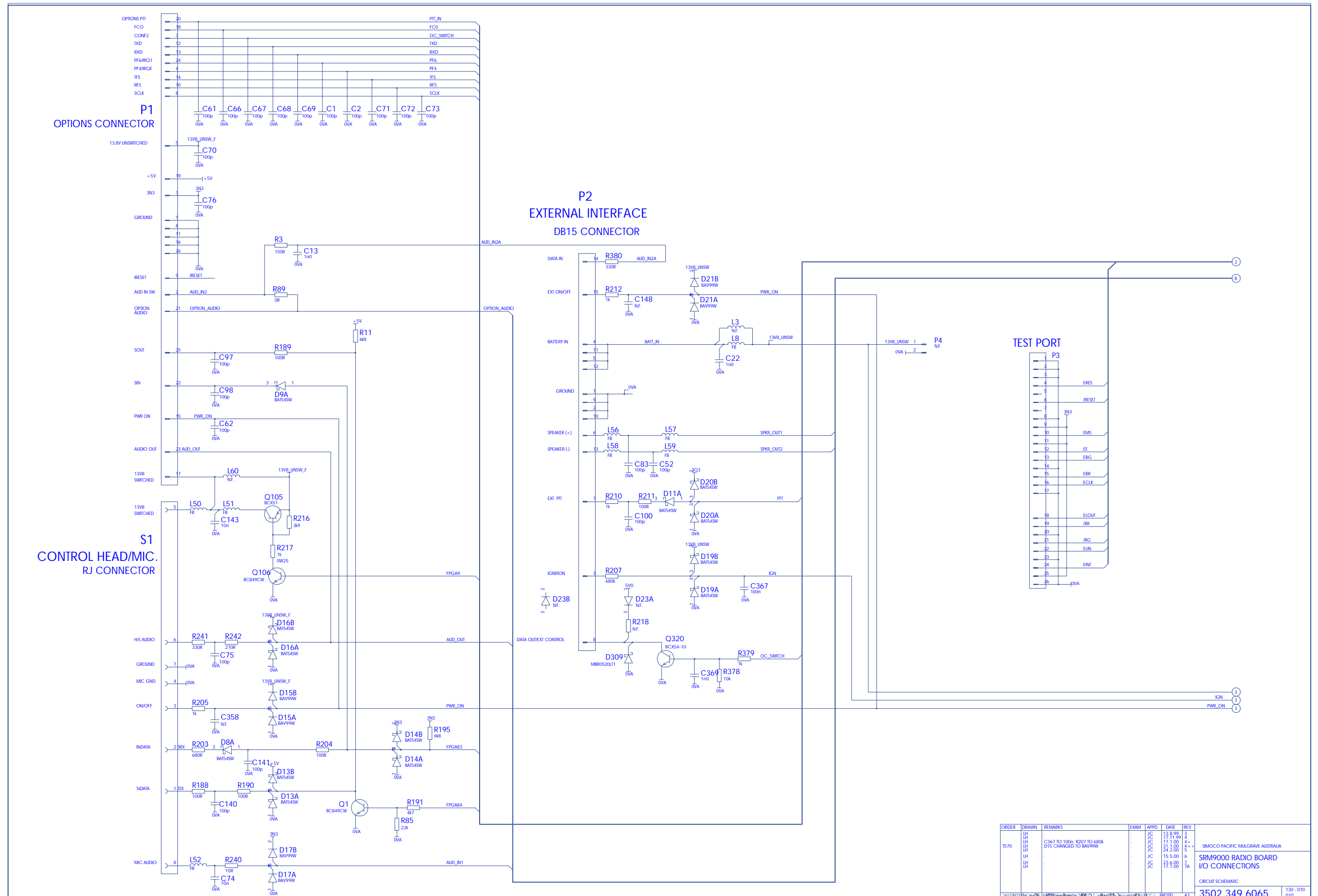


Figure 6 I/O Connections Schematic

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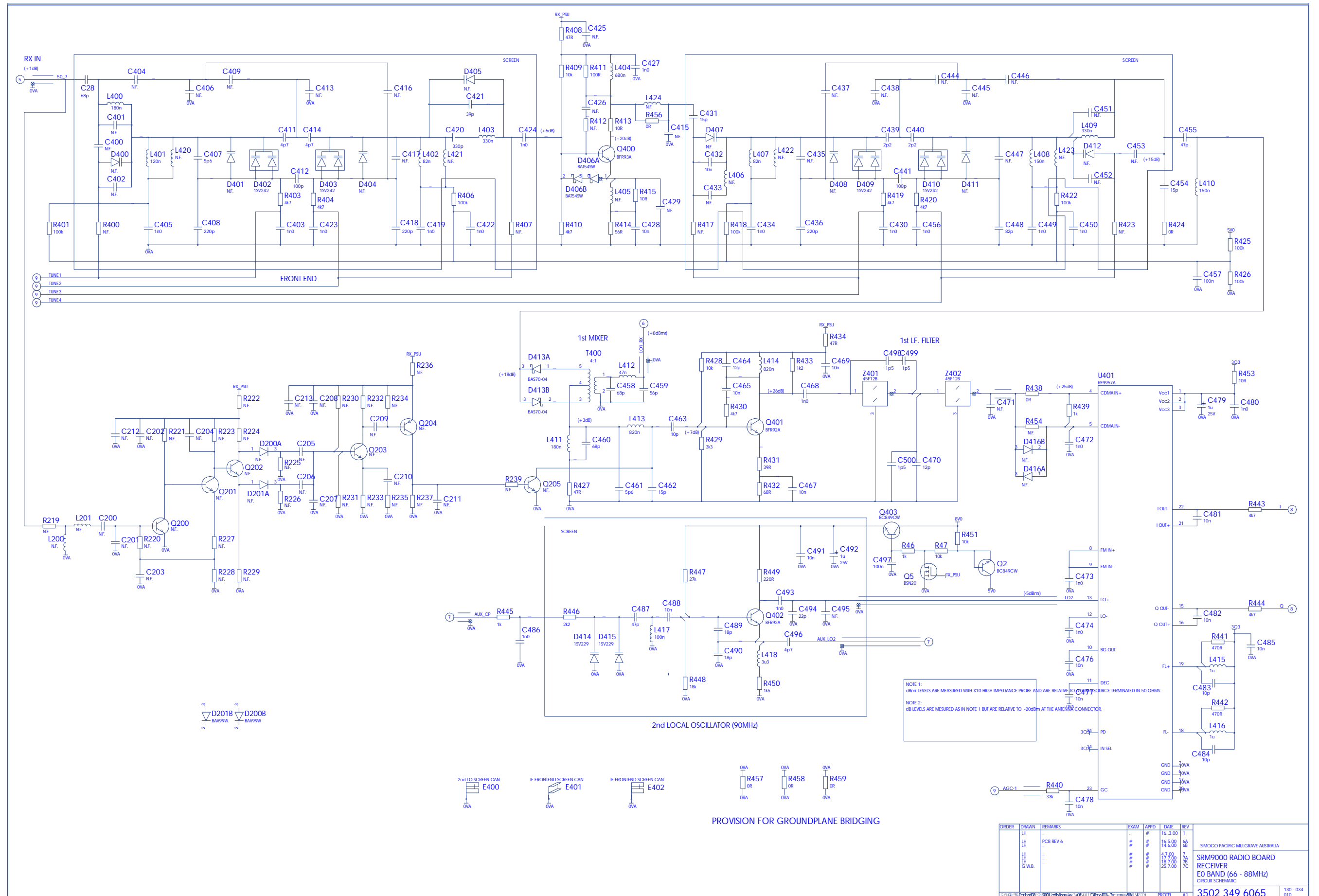


Figure 7 Reciever (EO Band) Schematic

Issue 7 Circuit Diagrams

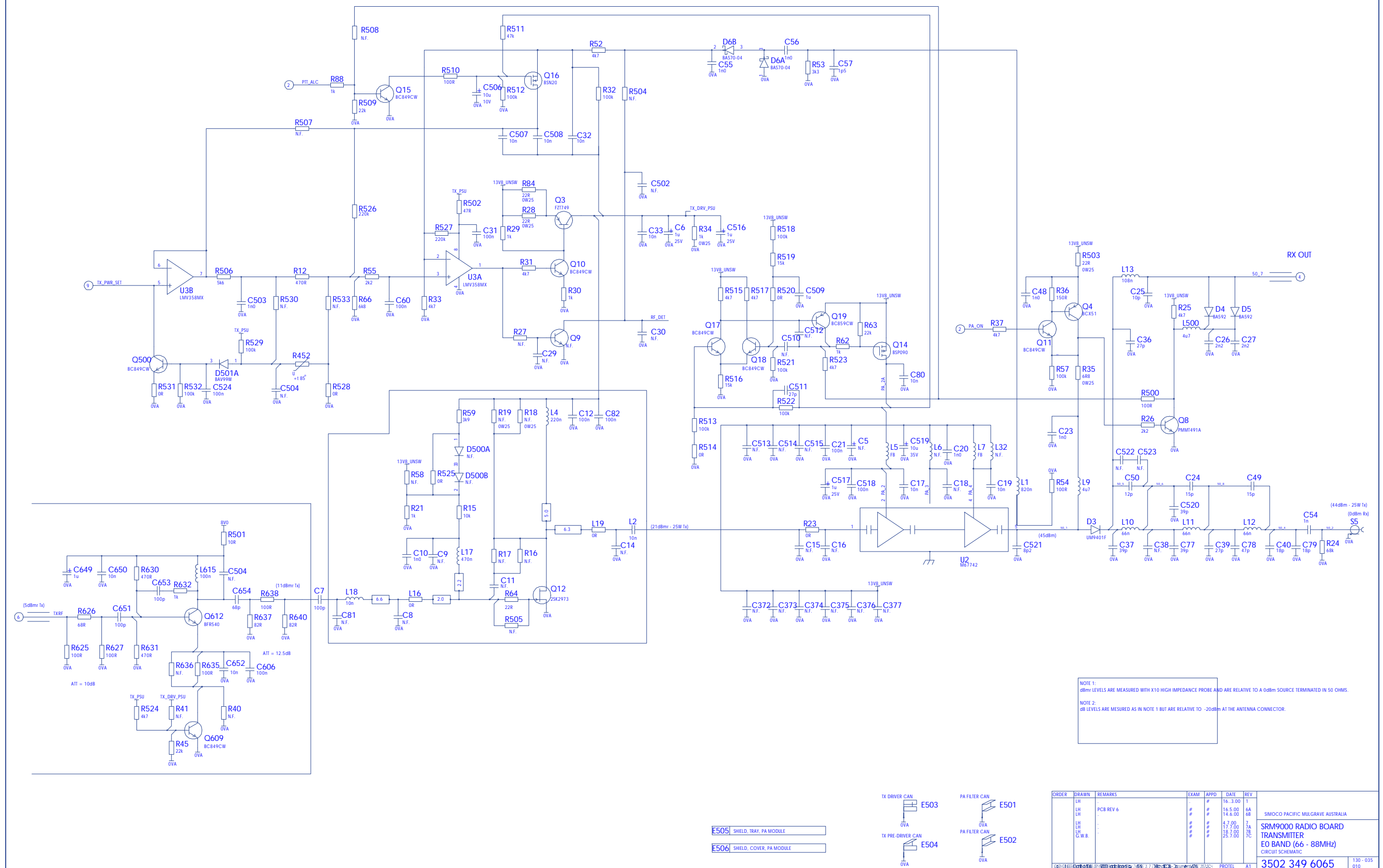


Figure 8 Transmitter (EO Band) Schematic

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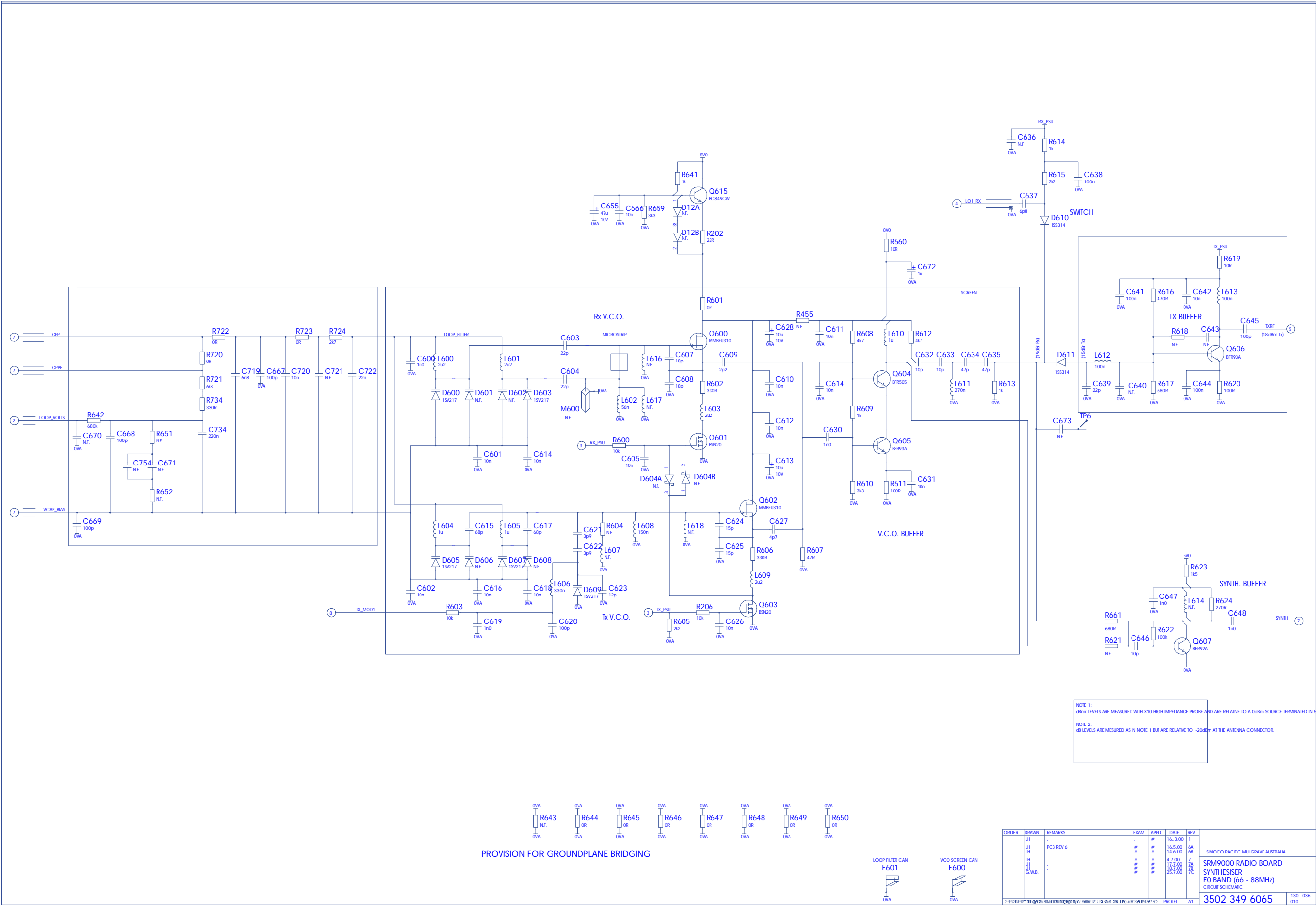


Figure 9 Synthesiser VCO (EO Band) Schematic

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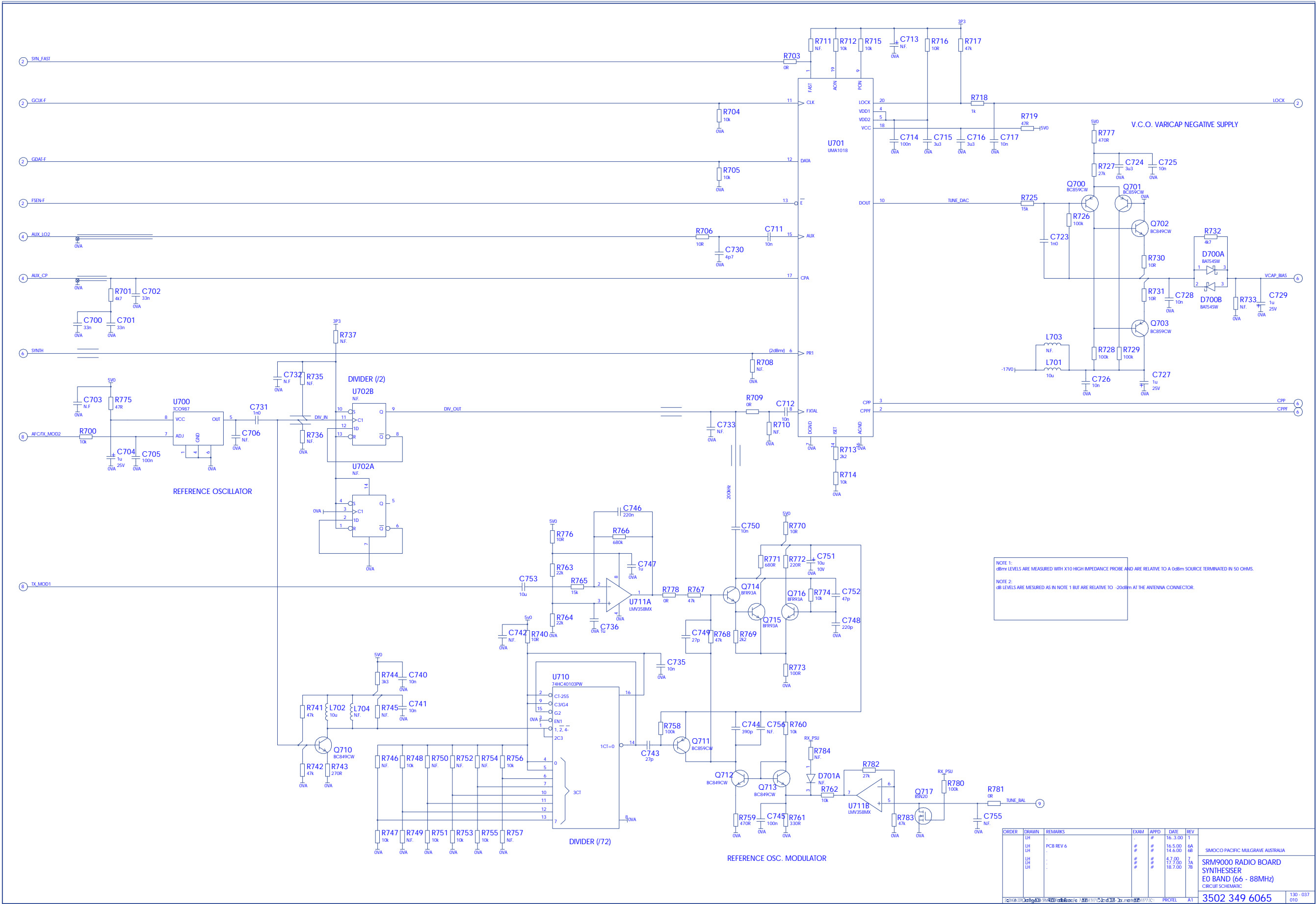


Figure 10 Synthesiser PLL (EO Band) Schematic

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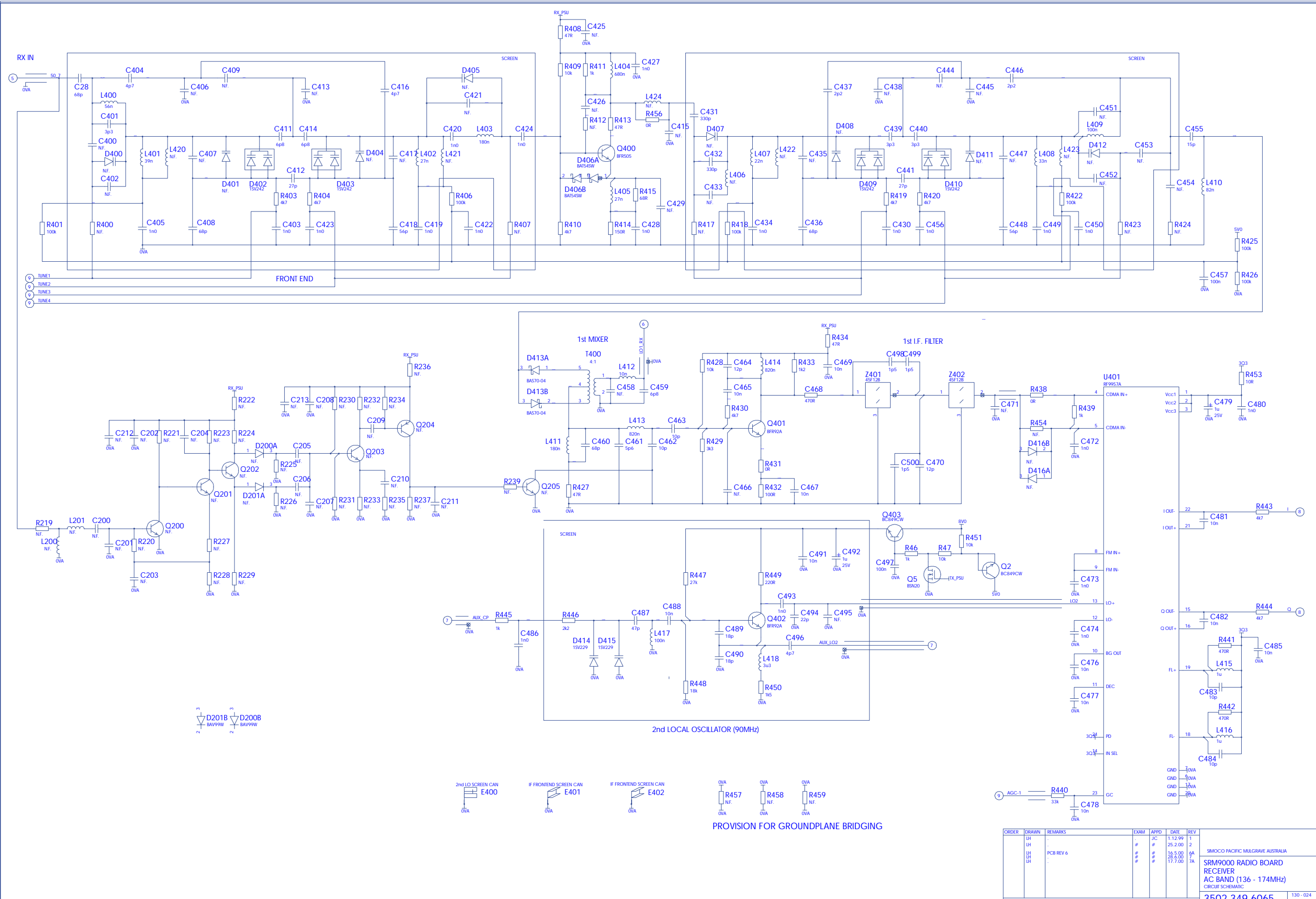


Figure 11 Receiver (AC Band) Schematic

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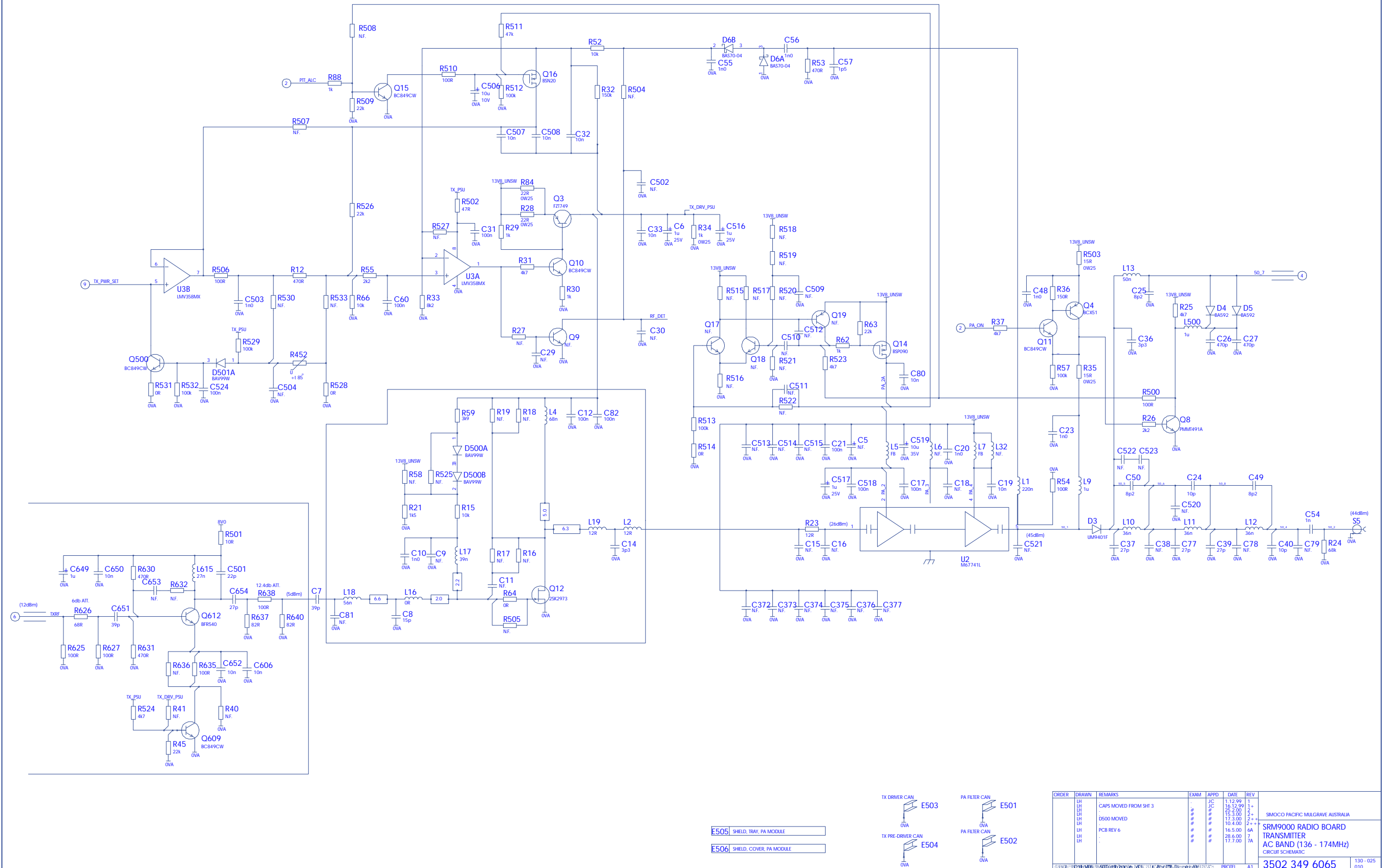


Figure 12 Transmitter (AC Band) Schematic

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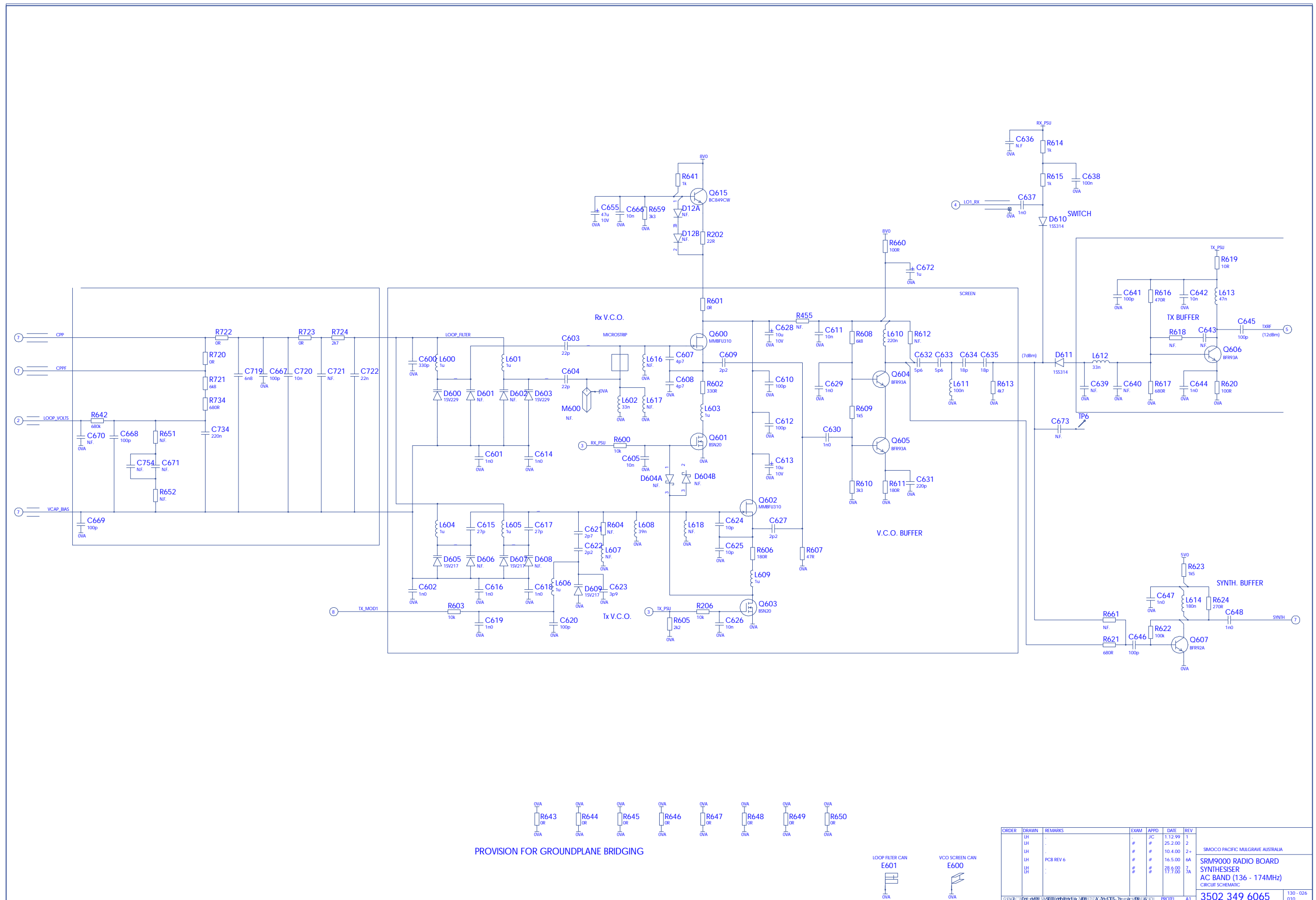


Figure 13 Synthesiser VCO (AC Band) Schematic

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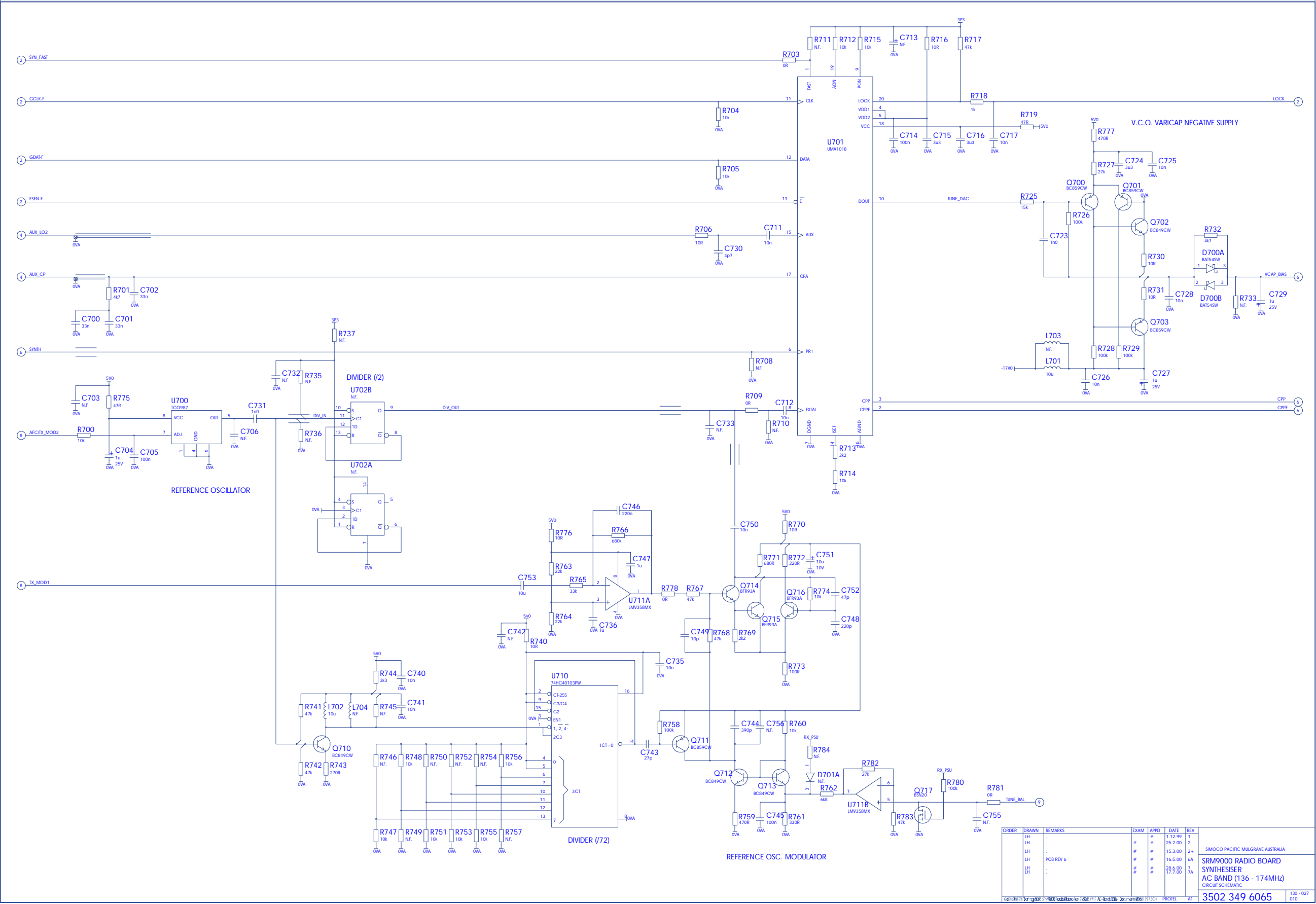


Figure 14 Synthesiser PLL (AC Band) Schematic

Issue 7 Circuit Diagrams

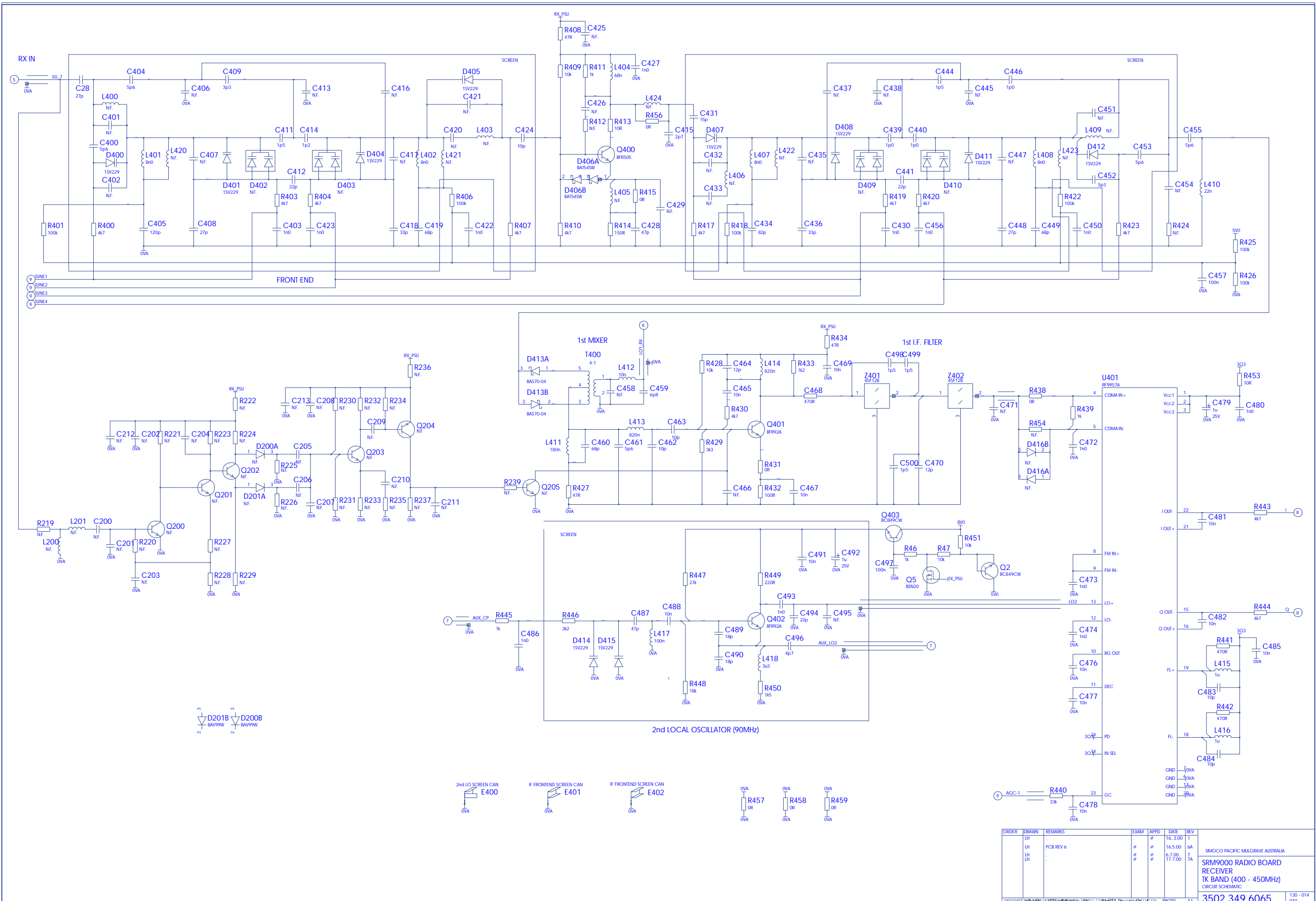


Figure 15 Receiver (TK Band) Schematic

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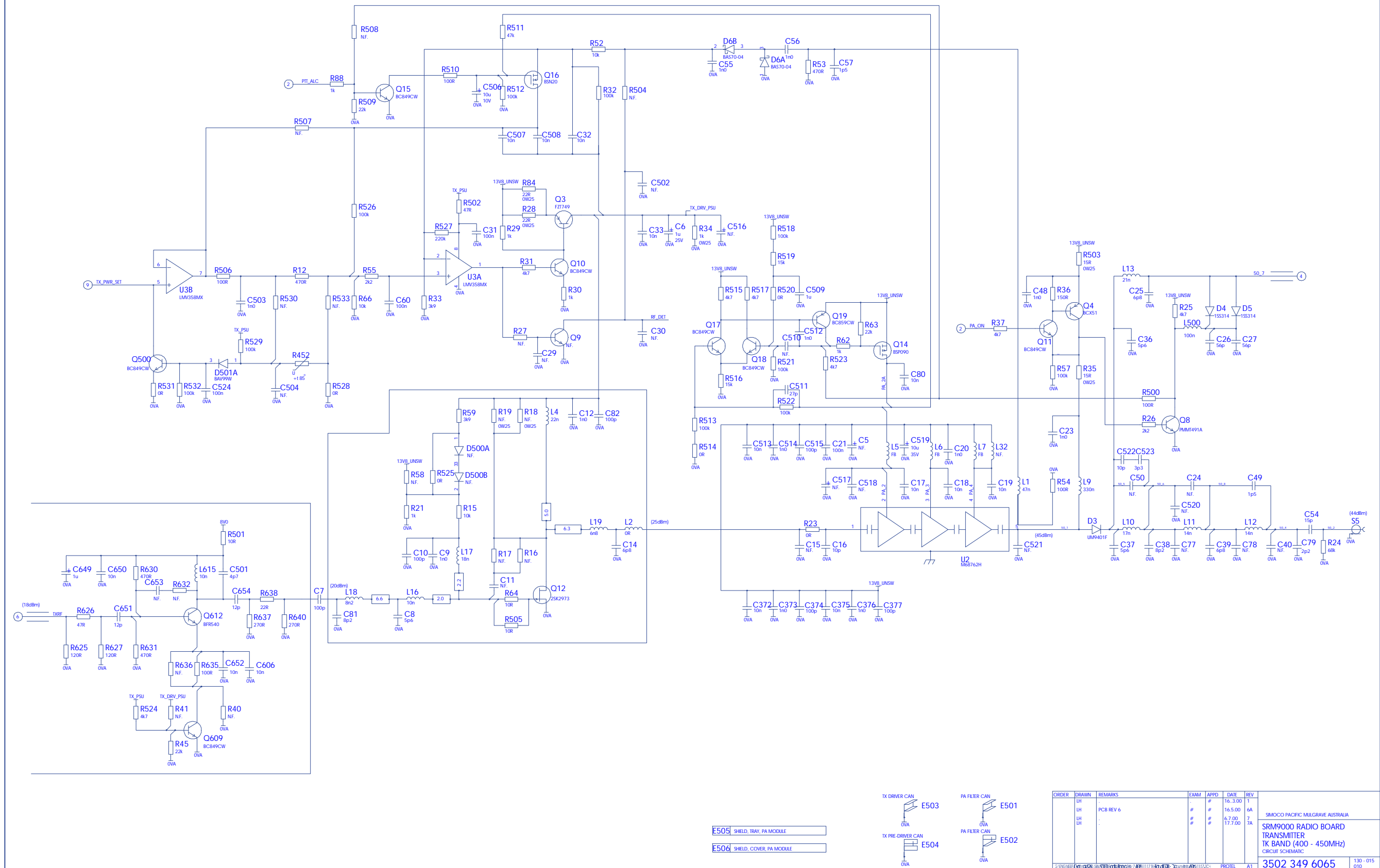


Figure 16 Transmitter (TK Band) Schematic

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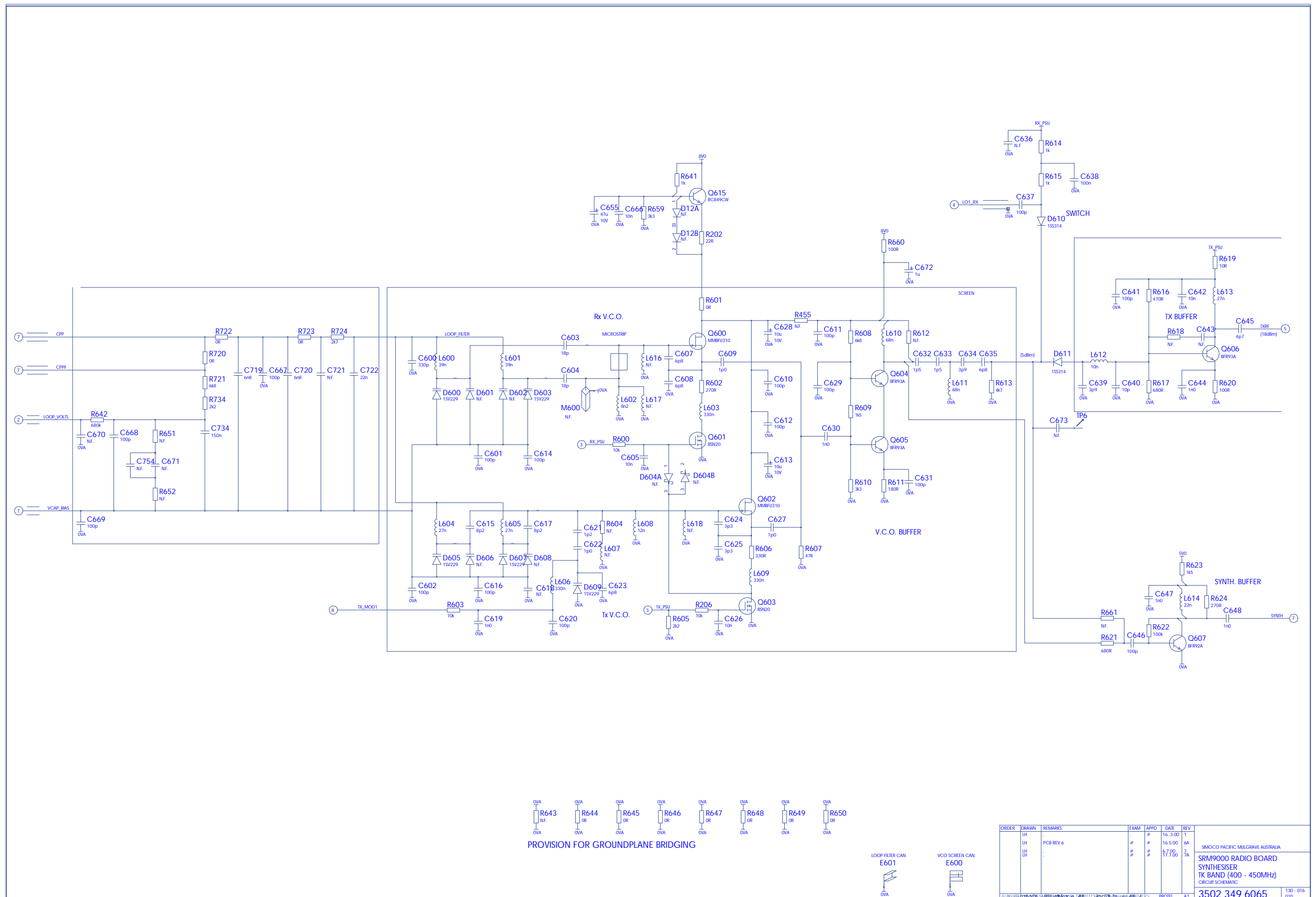


Figure 17 Synthesiser VCO (TK Band) Schematic

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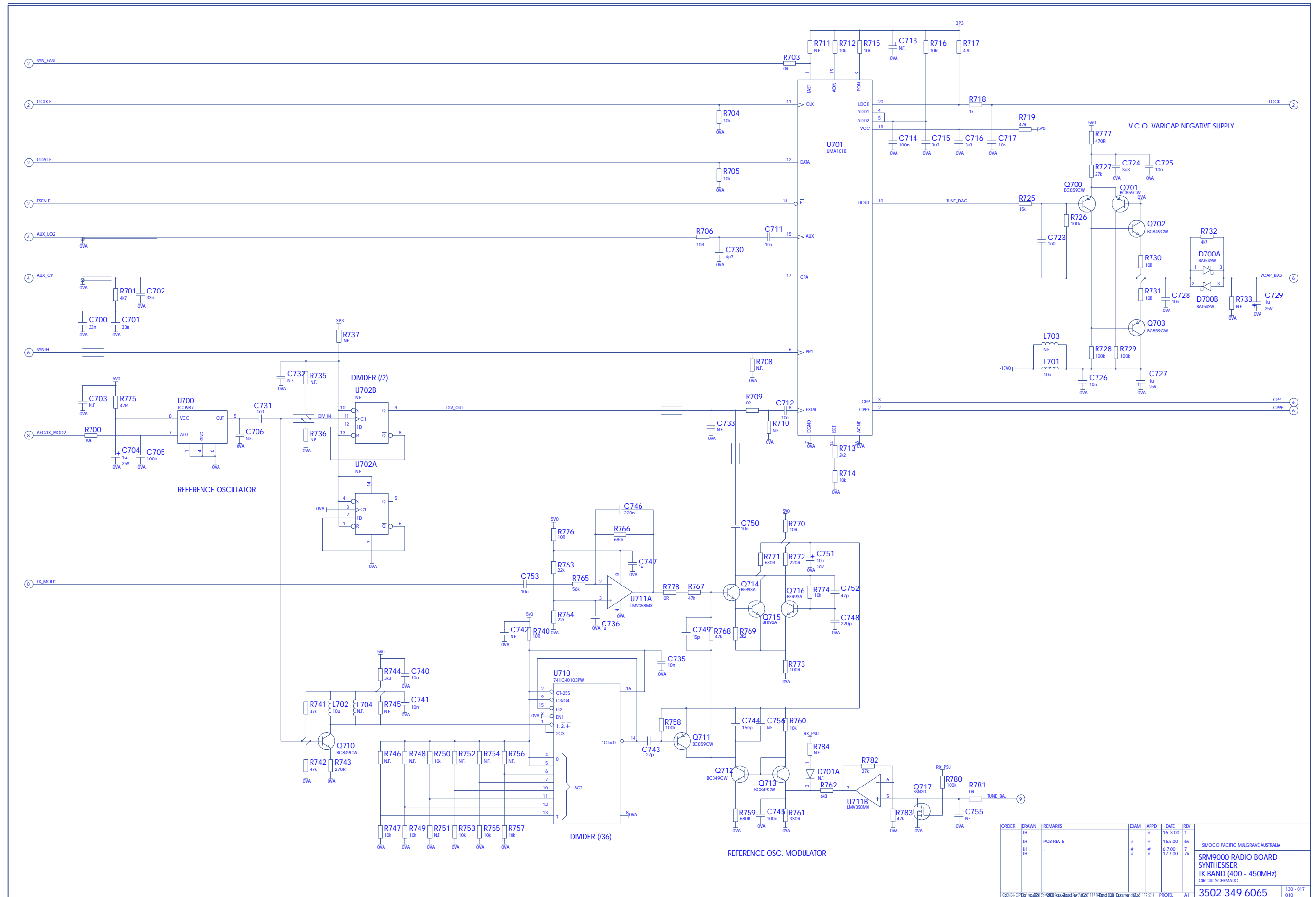


Figure 18 Synthesiser PLL (TK Band) Schematic

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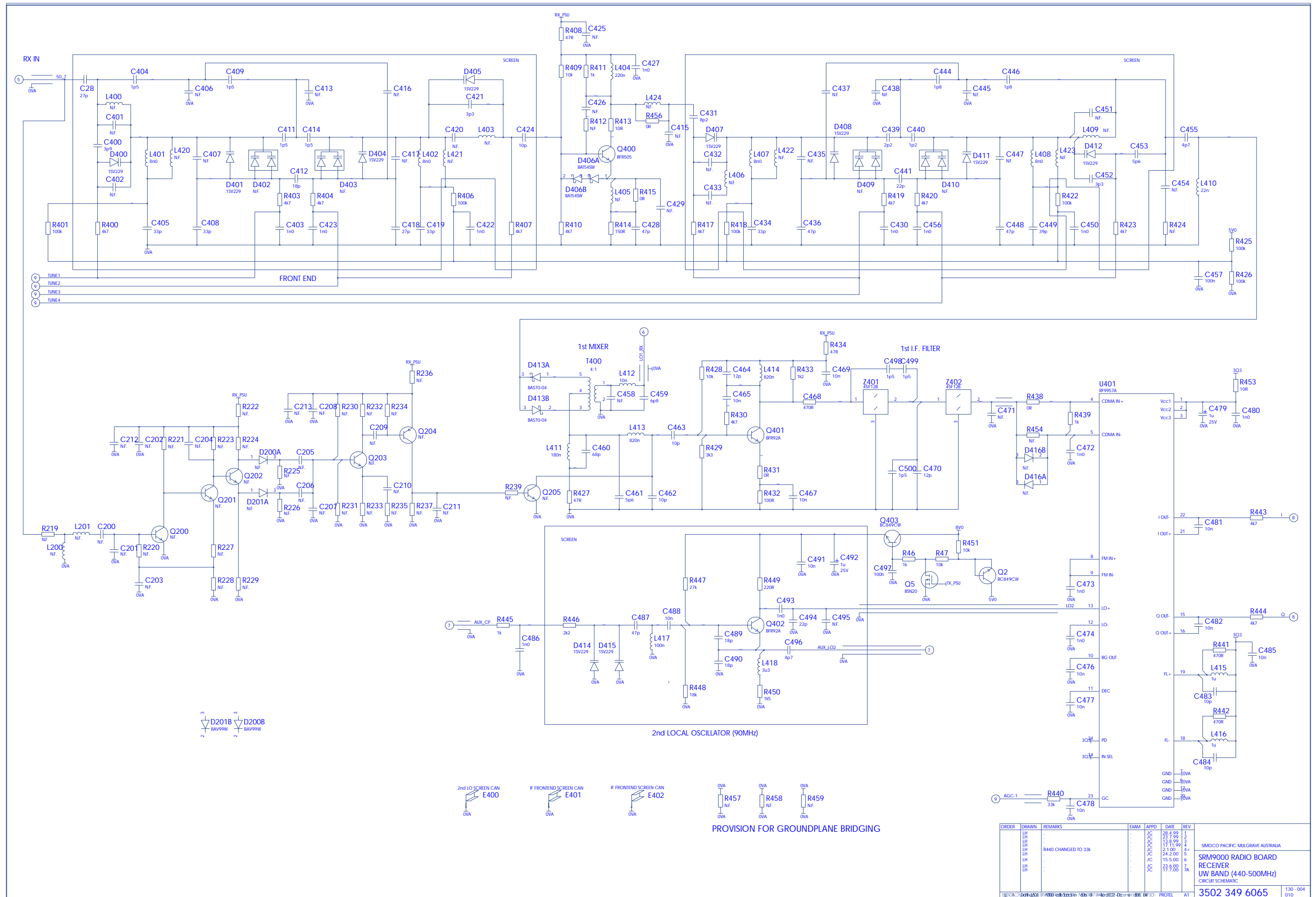


Figure 19 Receiver (UW Band) Schematic

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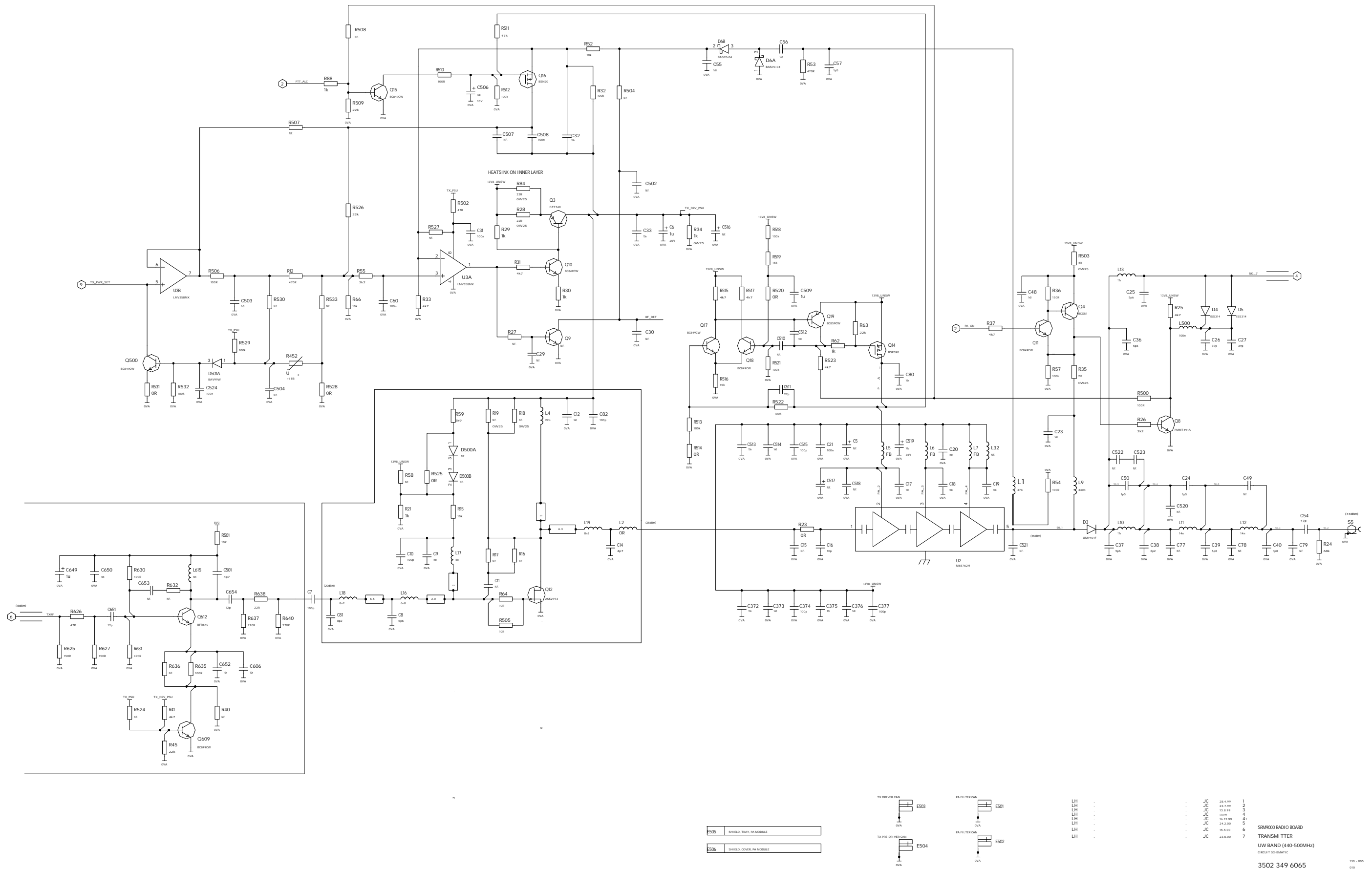


Figure 20 Transmitter (UW Band) Schematic

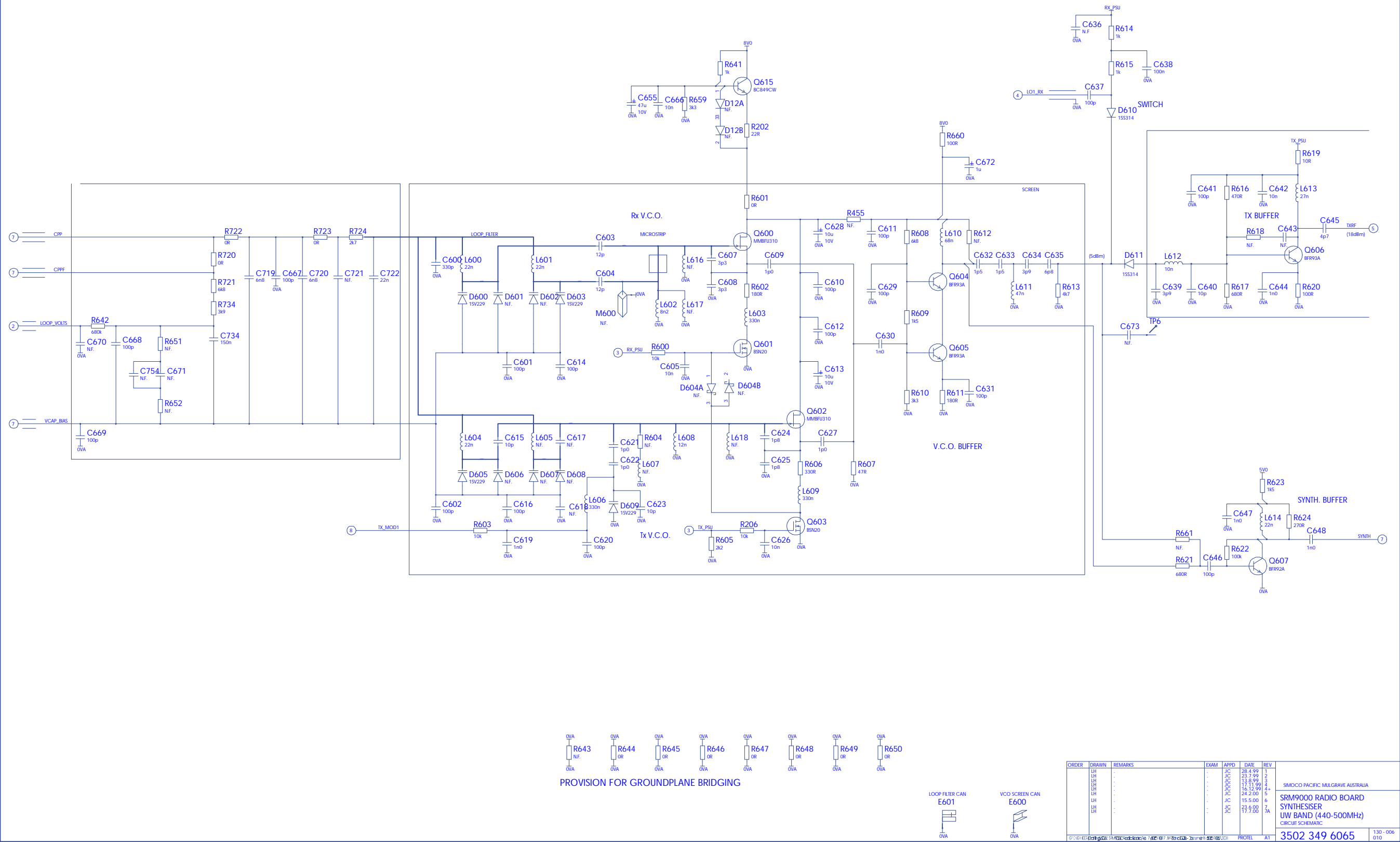


Figure 21 Synthesiser VCO (UW Band) Schematic

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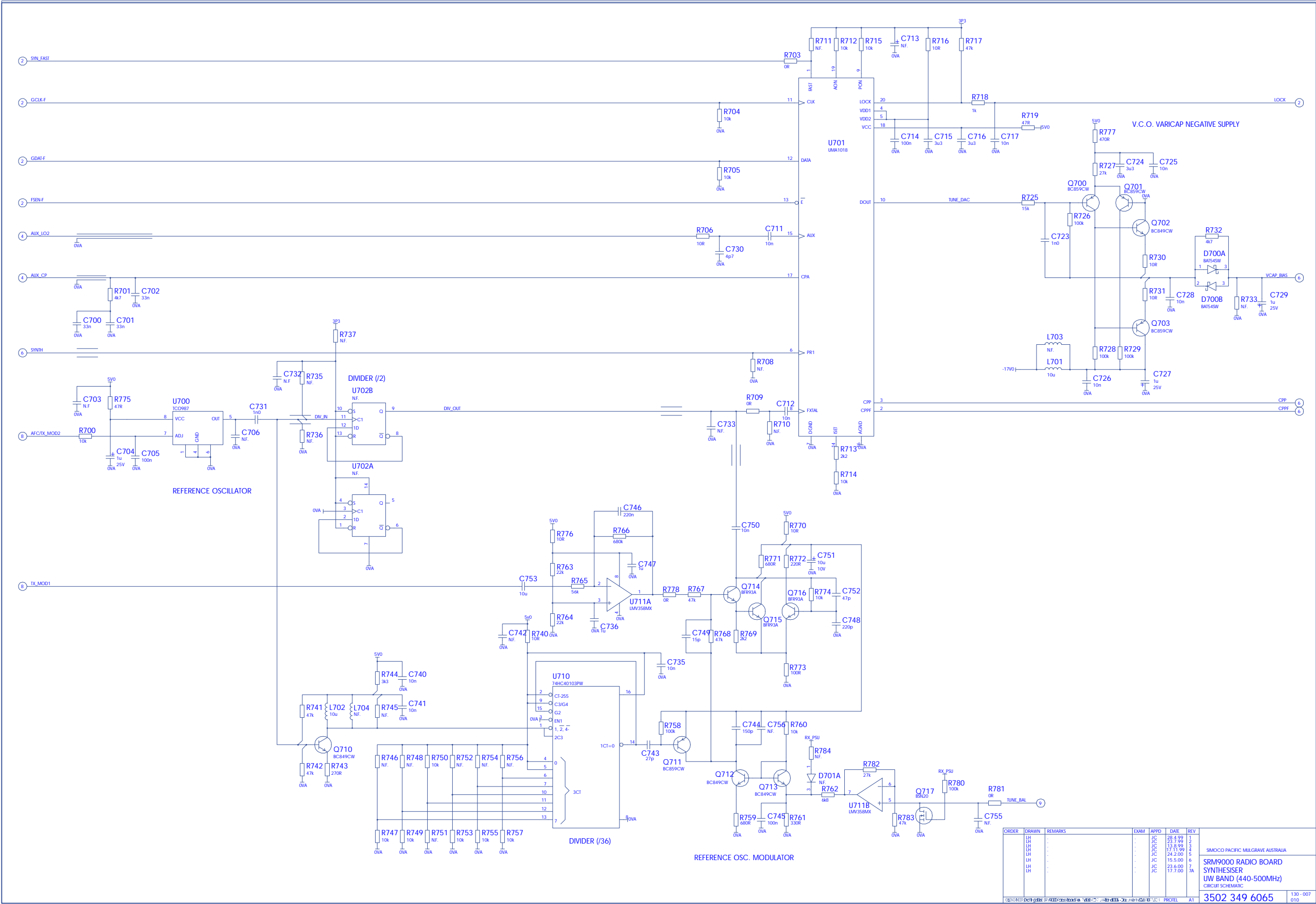


Figure 22 Synthesiser PLL (UW Band) Schematic

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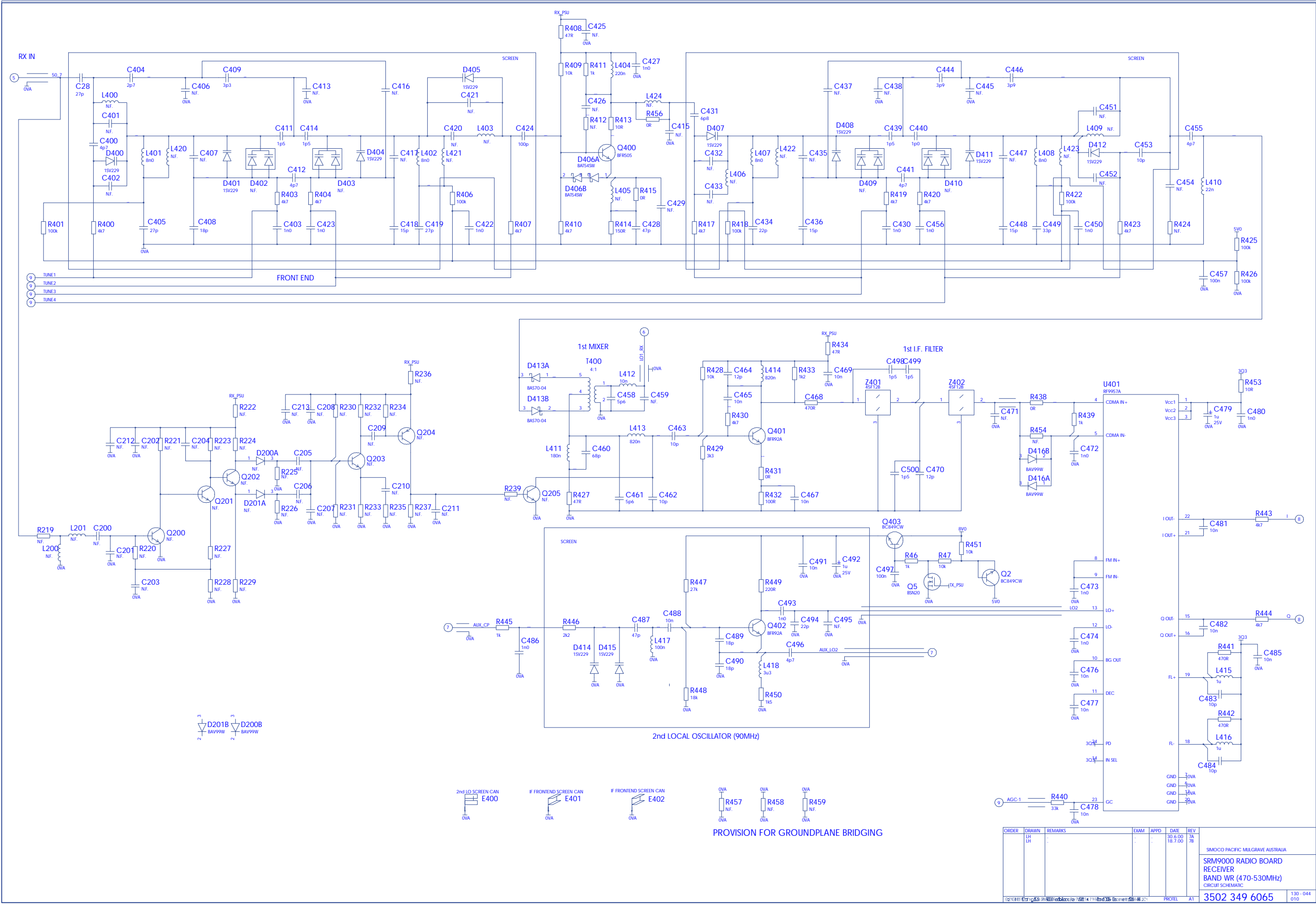


Figure 23 Receiver (WR Band) Schematic

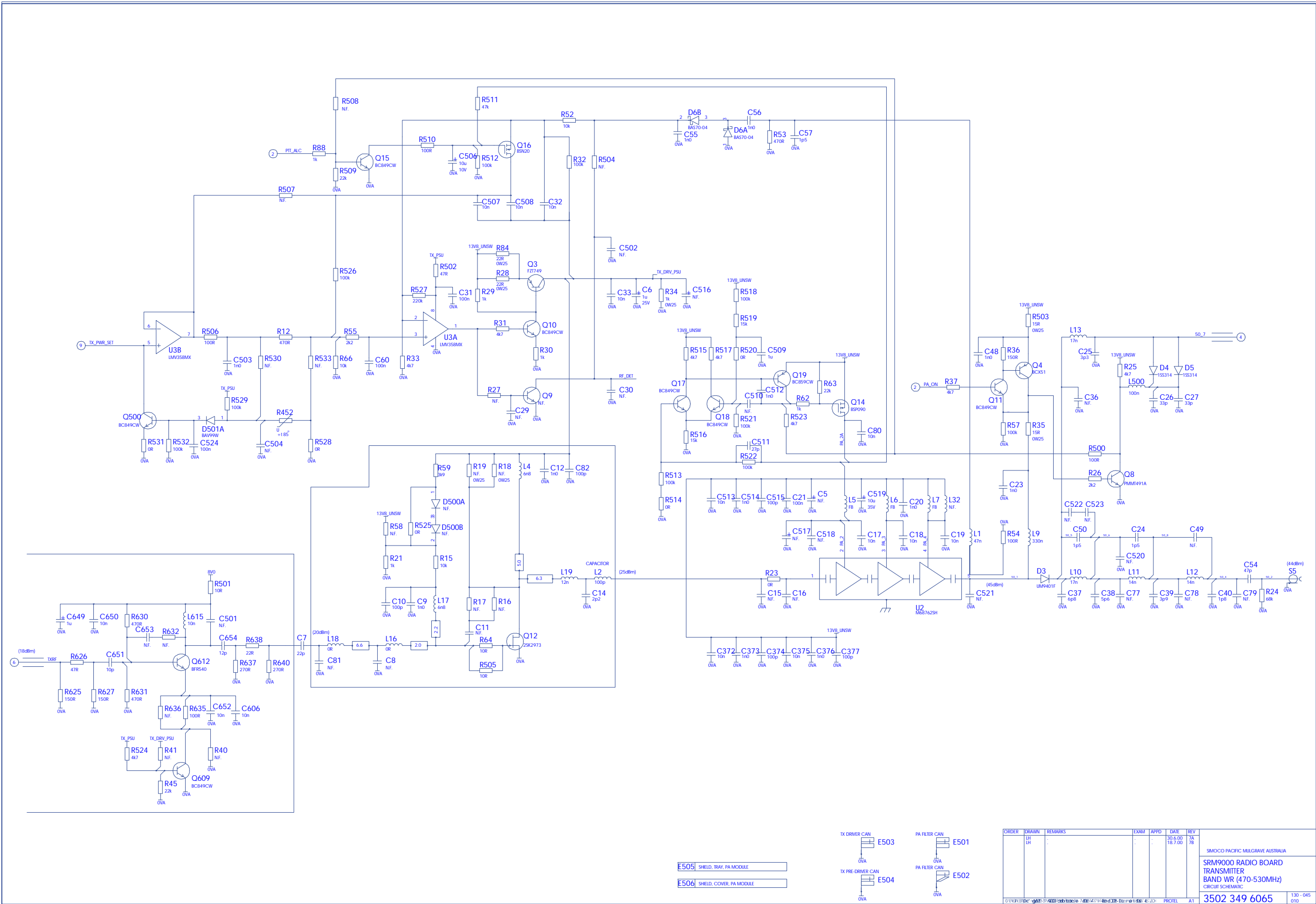


Figure 24 Transmitter (WR Band) Schematic

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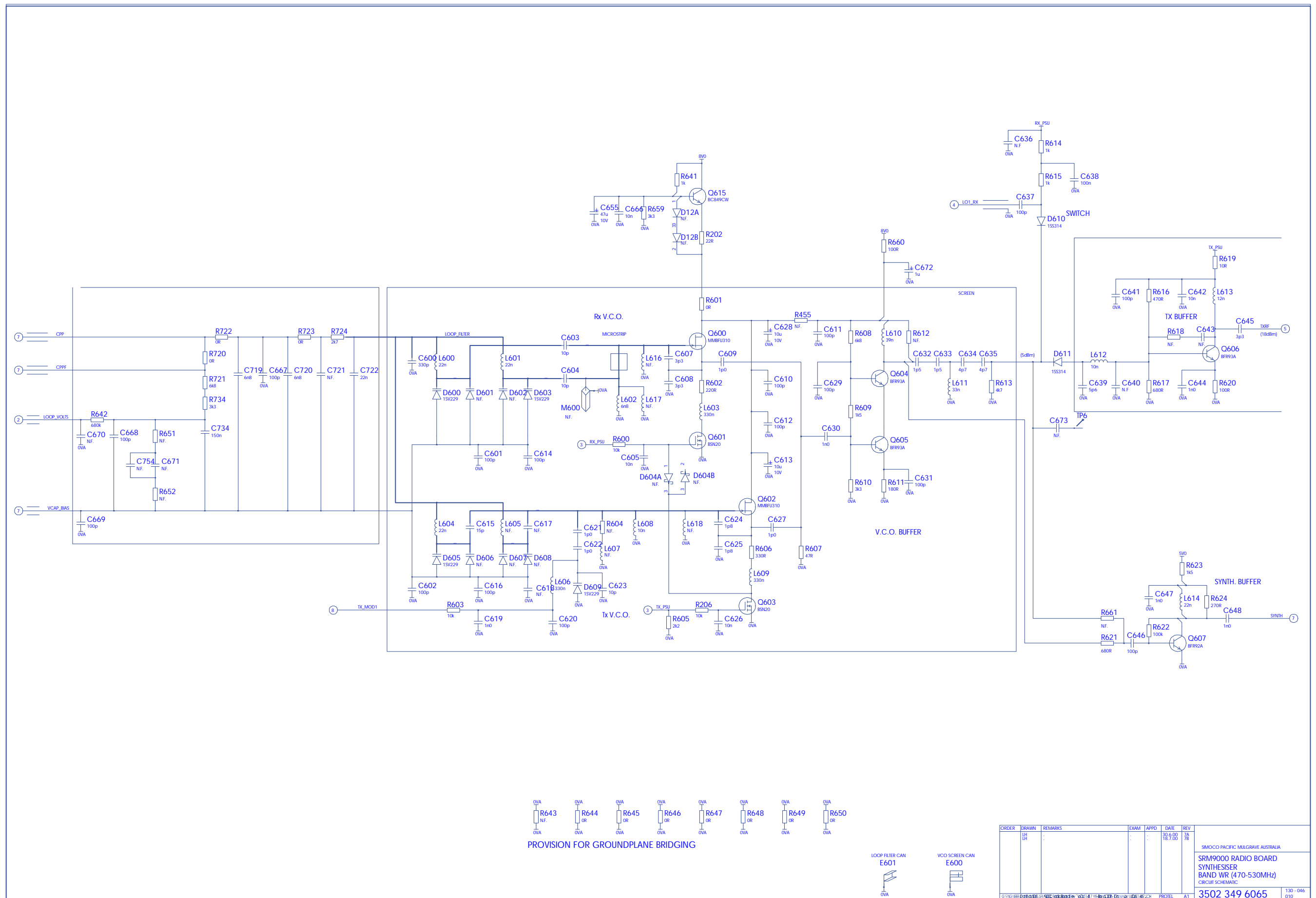


Figure 25 Synthesiser VCO (WR Band) Schematic

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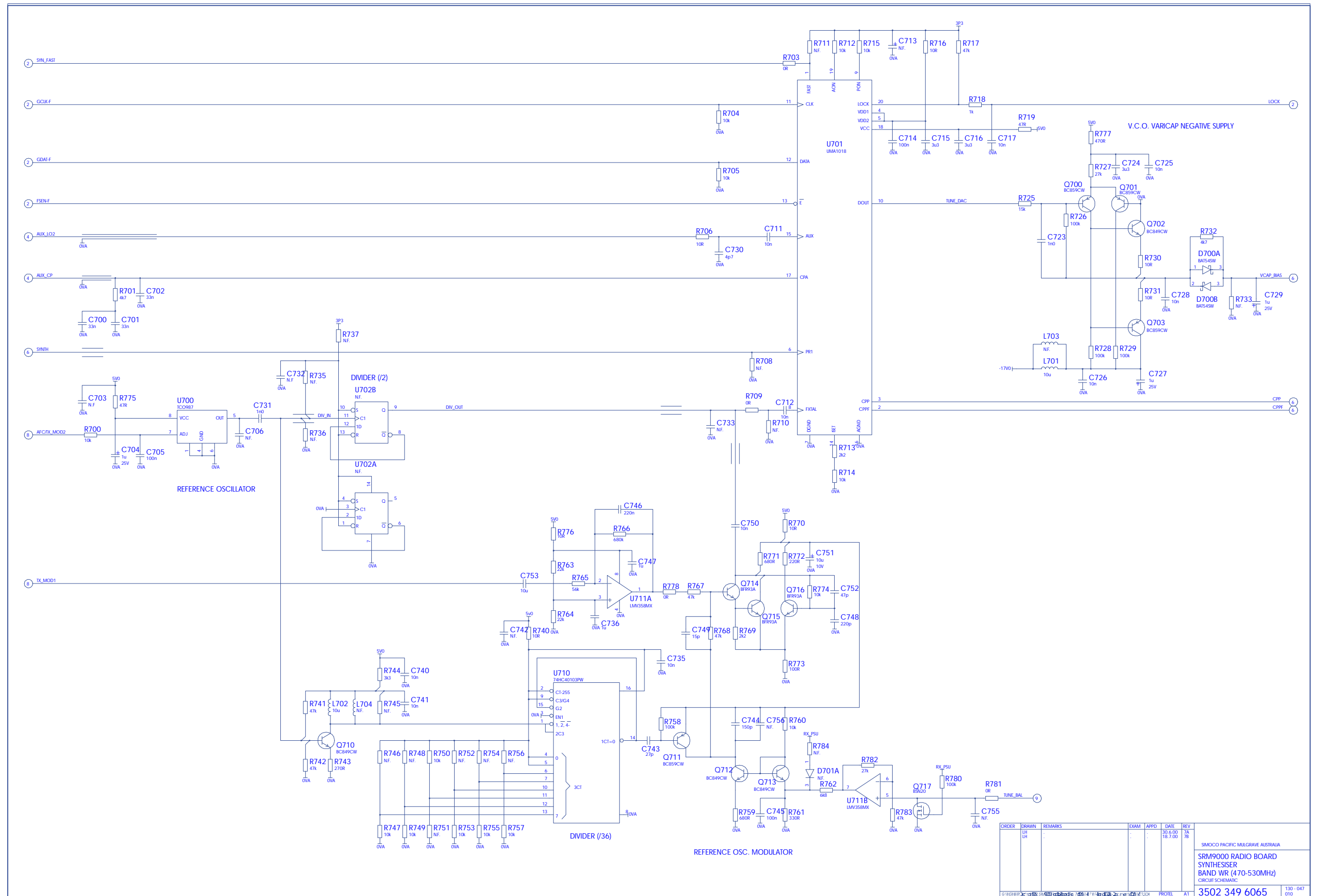


Figure 26 Synthesiser PLL (WR Band) Schemati

Issue 7 Circuit Diagrams

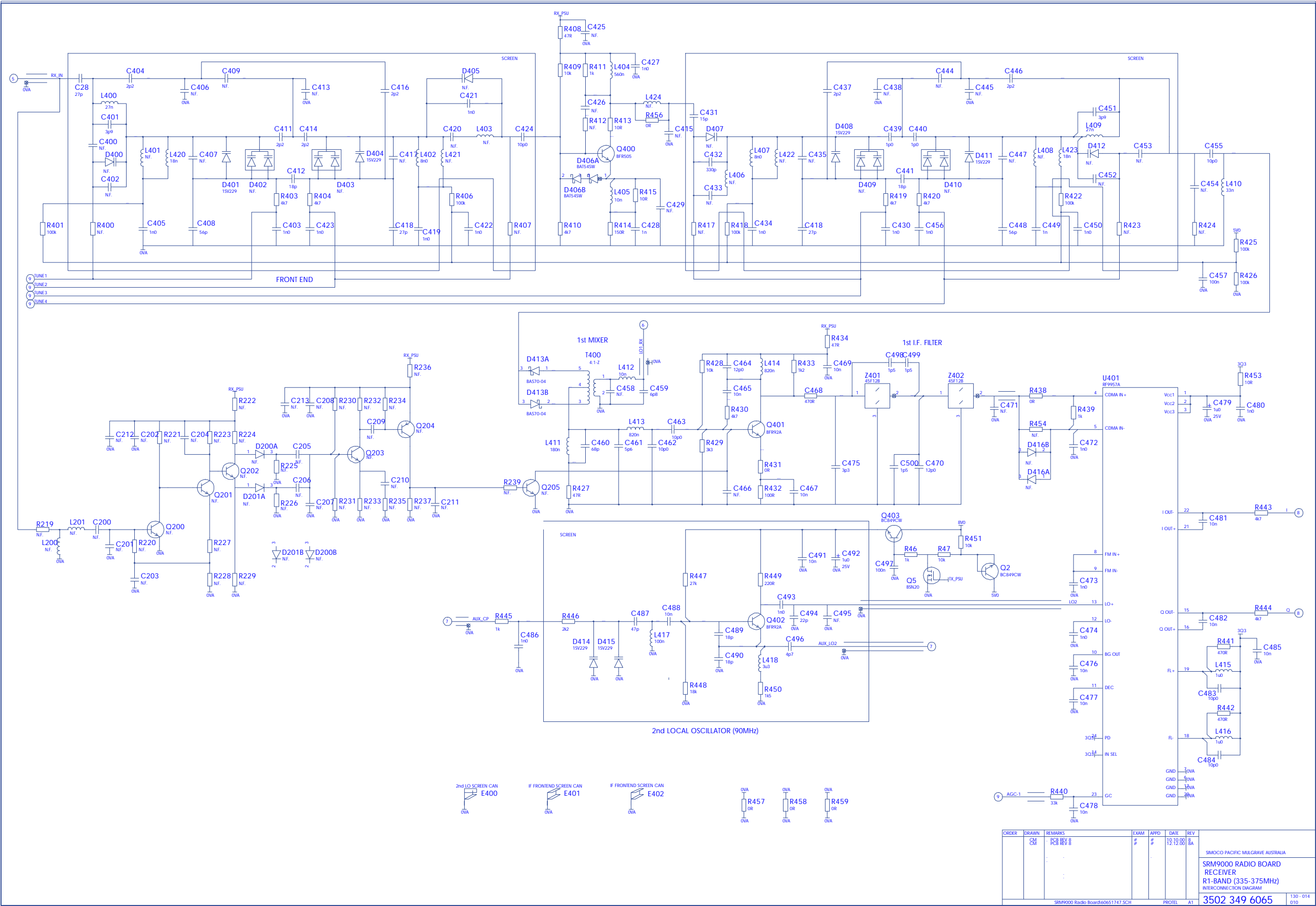


Figure 27 Receiver (R1 Band) Schematic

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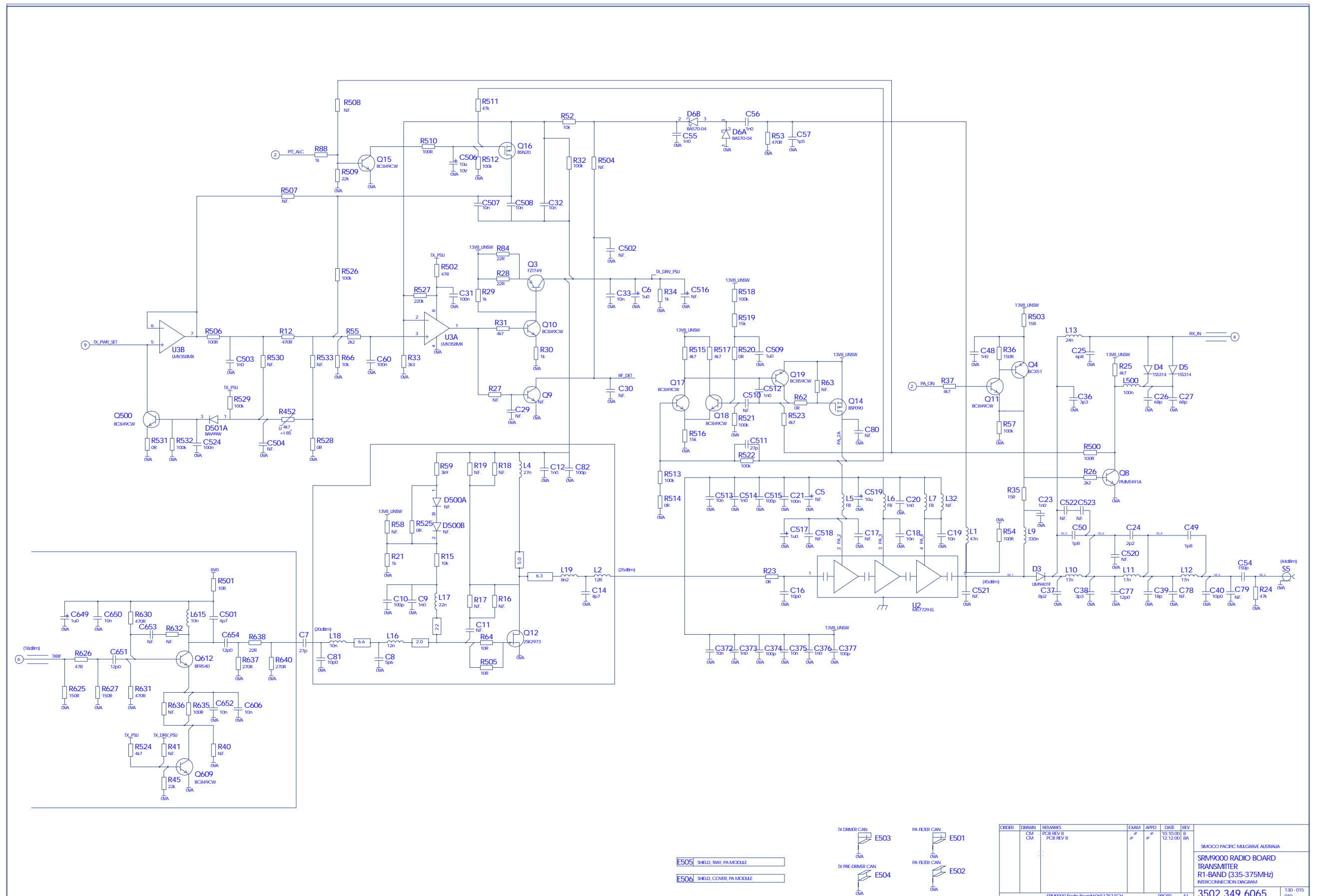


Figure 28 Transmitter (R1 Band) Schematic

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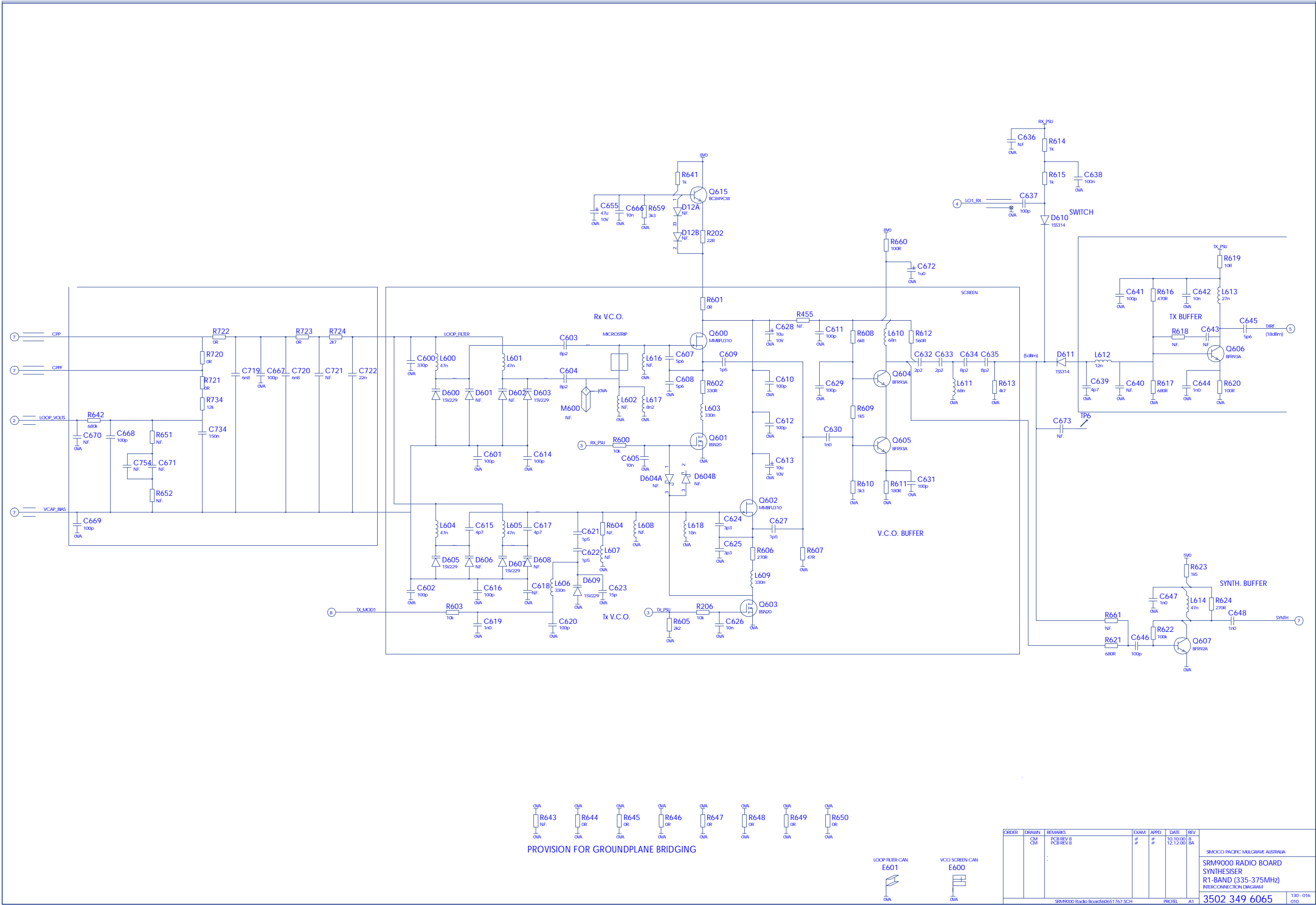


Figure 29 Synthesiser VCO (R1 Band) Schematic

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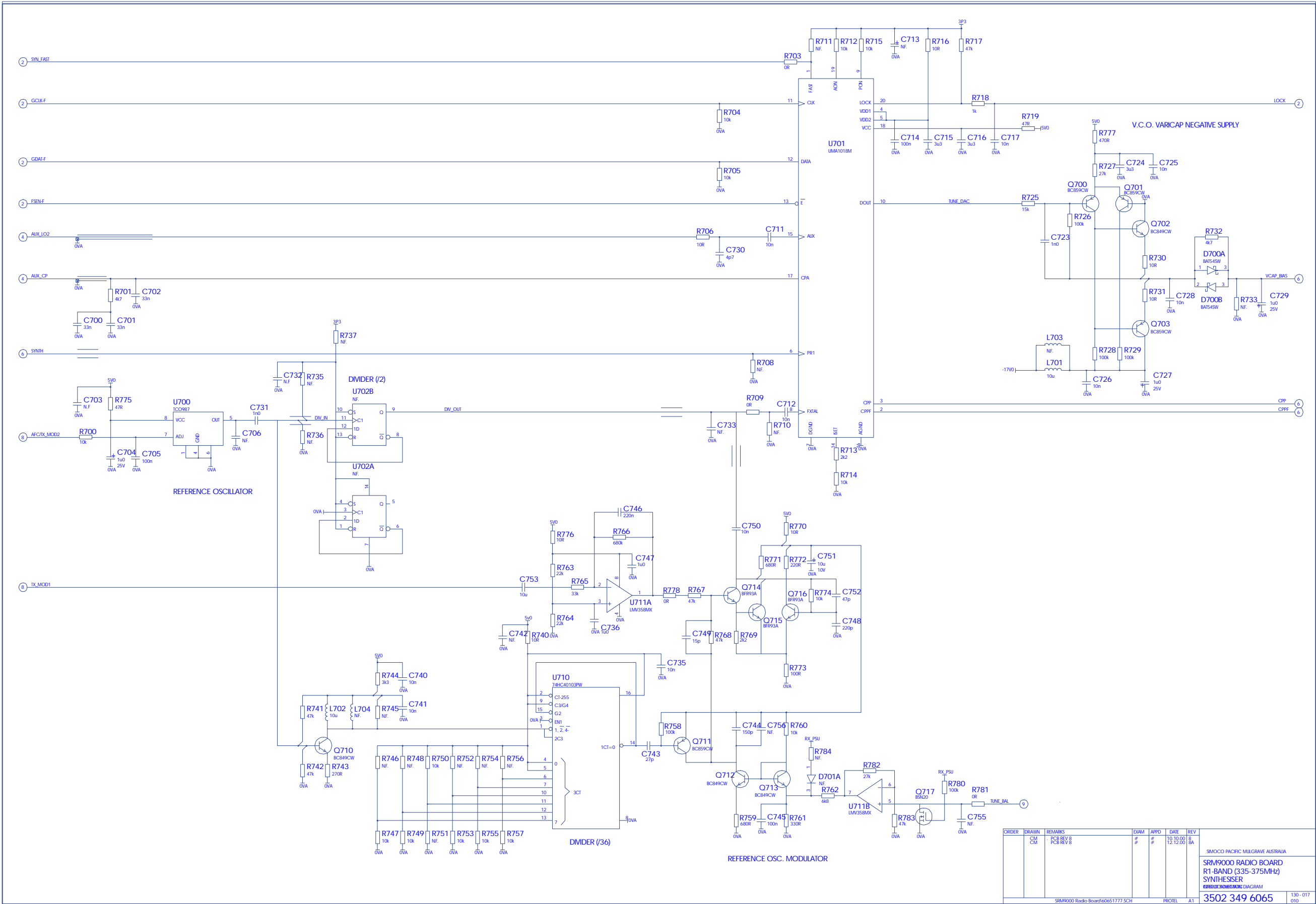


Figure 30 Synthesiser PLL (R1 Band) Schematic

DO NOT SCALE DIMENSIONS IN mm

COMPONENT LIST

ORDER	DRAWN	CHKD	AMMENDMENT	EXAM	APPD	DATE	REV
	LH				JC	16.8.99	3
	LH				JC	17.11.99	4
	LH				JC	1.5.00	5
	LH				JC	25.5.00	6
	LH				JC	23.6.00	7

UNLESS OTHERWISE STATED

TOLERANCES:

- WITHOUT DEC. POINT: ± 0.15
- WITH 1 DEC. PLACE: ± 0.15
- WITH 2 DEC. PLACES: ± 0.15
- ANGULAR: $\pm 0.5^\circ$

SCALE: 1:1

MATERIAL:

FINISH:

P/N:

SUPERSCEDES:

3502 349 6065

COMPONENT LAYOUT TOP SIDE/TOP

SRM9000 RADIO BOARD

simoco

110/002 OF 004

60658017.DWG

ACAD A2

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DO NOT SCALE
DIMENSIONS
IN mm

MATERIAL:
FINISH:
P/N:
SUPERCEDES:

UNLESS OTHERWISE STATED
TOLERANCES:
WITHOUT DEC. POINT: ± 0.15
WITH 1 DEC. PLACE: ± 0.15
WITH 2 DEC. PLACES: ± 0.15
ANGULAR: $\pm 0.5^\circ$
SCALE: 1:1

ORDER DRAWN CHKD AMMENDMENT
LH
LH
LH
LH
LH

EXAM APPD DATE REV
JC 16.8.99 3
JC 17.11.99 4
JC 1.5.00 5
JC 25.5.00 6
JC 23.6.00 7

SRM9000
RADIO BOARD
COMPONENT LAYOUT TOP SIDE/BOTTOM
3502 349 6065

SH 110/001
OF 004

60558017.DWG
ACAD A2

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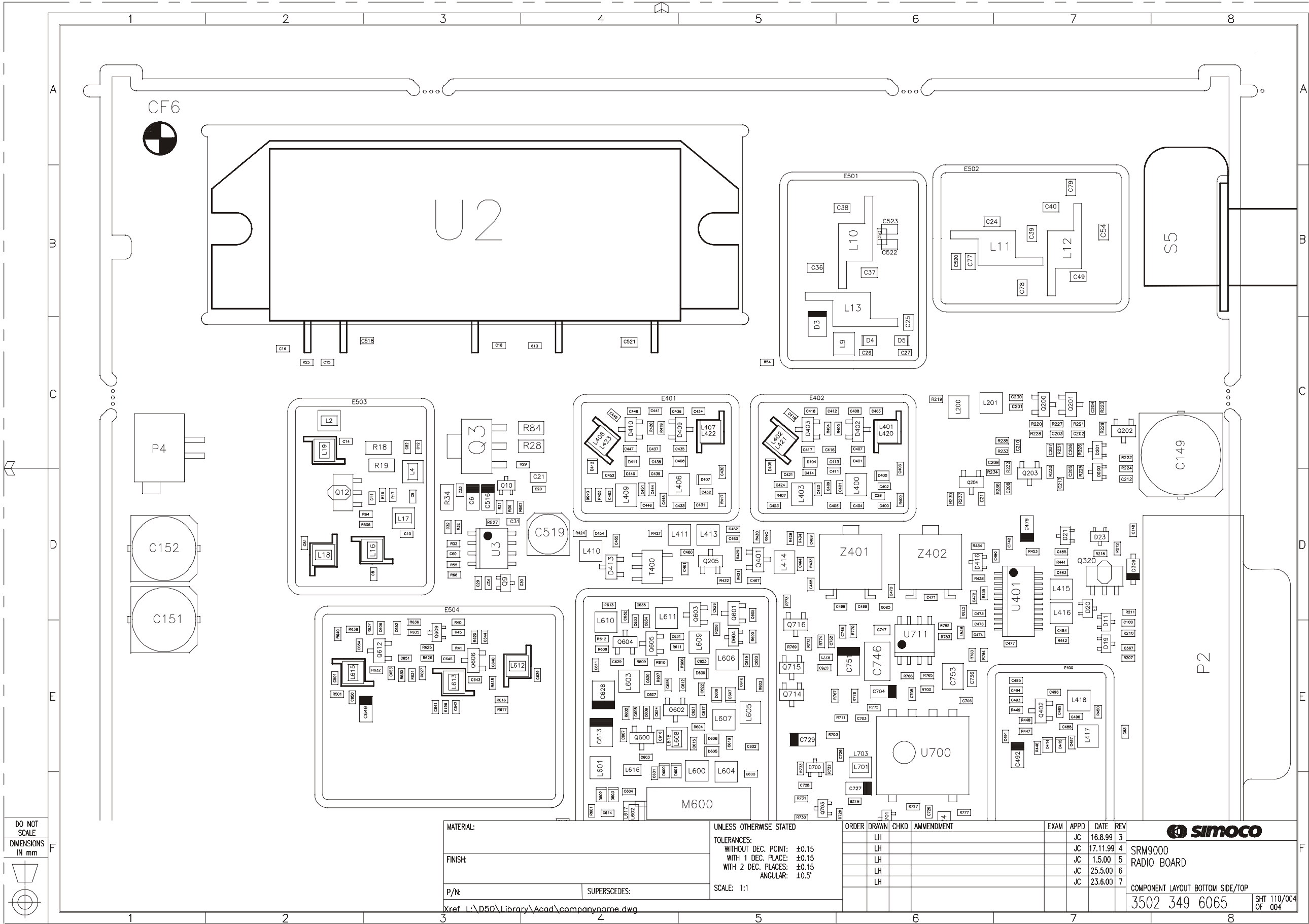


Figure 33 PCB Layout - Bottom side / Top

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