SRM9000 OPTION CONNECTORS

Applicable to models:

9005 PMR	9010 PMR	9020 PMR	9022 PMR	9025 PMR	9030 PMR
9005 Trunk	9010 Trunk	9020 Trunk	9022 Trunk	9025 Trunk	9030 Trunk

1. Introduction

This Application Note details the interface characteristics of radio connectors for all radio versions of SRM9000.

Several connectors are provided for option board and external interface purposes, the details of which are as follows:

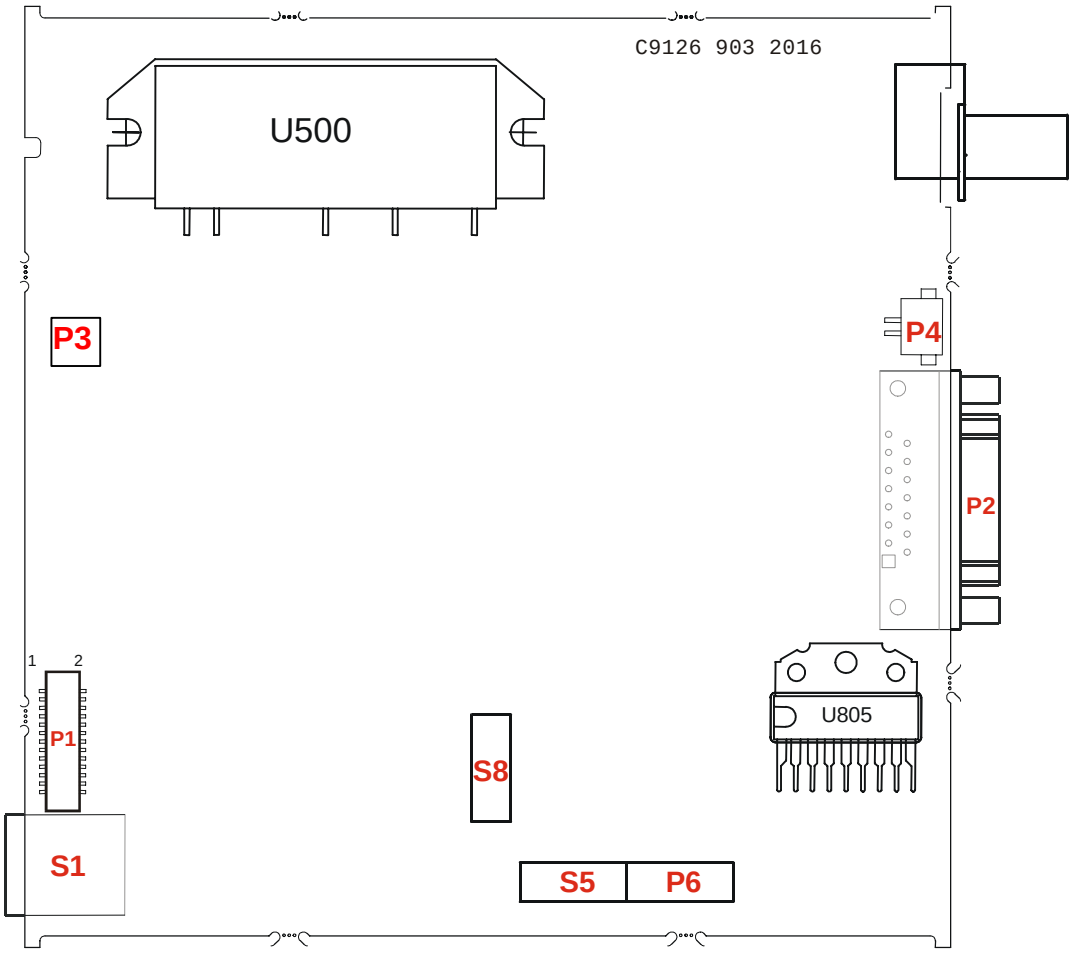


Figure 1.1 SRM9000 Connector Locations (Rev 9)

Note. P3, P4 normally not fitted. P4, S5, P6 and S8 are applicable to Rev 9+ only.

2. Connector Functionality

2.1 26 Way Header (Connector P1)

A 26 way miniature header mounted at the front edge of the PCB next to the front RJ8 connector. This header is the means of interfacing the radio PCB with several internally installed Option PCBs.

Two versions of this header exist:

Radio PCBs of Revision 7 and earlier (~prior to July 2001) have a right-angle horizontal header.

Radios using Revision 8 and later PCBs have a vertical header.

The vertical orientation allows for the small Option-Boards, (eg. Systems-Interface-Board [Encryption], etc.) to be directly mounted. This also stops accidental fitting of these options without the necessary modifications.

The larger Option PCBs can also have the ability to provide additional external interface functions.

The Pin-out functions on the 26-way Options Header vary, depending on which “Option Board” is selected in the Jobfile (setup by the Programmer - See below for details showing how to select different boards).

Shown below is the function of each line for the various possible selections.

The Table below shows the differences between the different revisions of PCBs.

2.1.1 Pin-out differences between Rev 7, 8 and 9 PCB Versions

Pin No	Rev 9 - Function name	Rev 8 - Function Name	Rev 7- Function Name
1	Ground	Ground	Ground
2	Aud In / CCLK	Aud In / CCLK	Aud In
3	CLRC	CLRC	3N3
4	PF4	PF4 / IRQE	PF4 / IRQE
5	13.8V Unswitched	13.8V Unswitched	13.8V Unswitched
6	CONF2	CONF2	Ground
7	13.8V Unswitched	13.8V Unswitched	CONF2
8	SCLK	SCLK	SCLK
9	IRESET	IRESET	IRESET
10	RFS	RFS	RFS
11	L3C	L3C	Ground
12	TxD	TxD	TxD
13	RxD	RxD	RxD
14	TFS	TFS	TFS
15	Audio / PWR ON	Audio / PWR ON	PWR ON
16	L3D	L3D	Ground
17	13.8V Switched	13.8V Switched	13.8V Switched
18	FC0	FC0 /Optional Connection	FC0
19	L3M	L3M	+5V
20	Options PTT	Options PTT	Options PTT
21	Option Audio	Option Audio	Option Audio
22	SIN	SIN	SIN
23	Audio Out	Audio Out	Audio Out
24	PF6	PF6 / IRQ1	PF6 / IRQ1
25	SOUT	SOUT	SOUT
26	Ground	Ground	Ground

2.1.2 Option Board Selection in the Programmer

The radio SW needs to know which Option-Board is fitted so it can correctly interface to it via the Header connections.
The type of Option-Board can be selected as shown below (using FPP Version 5.09).

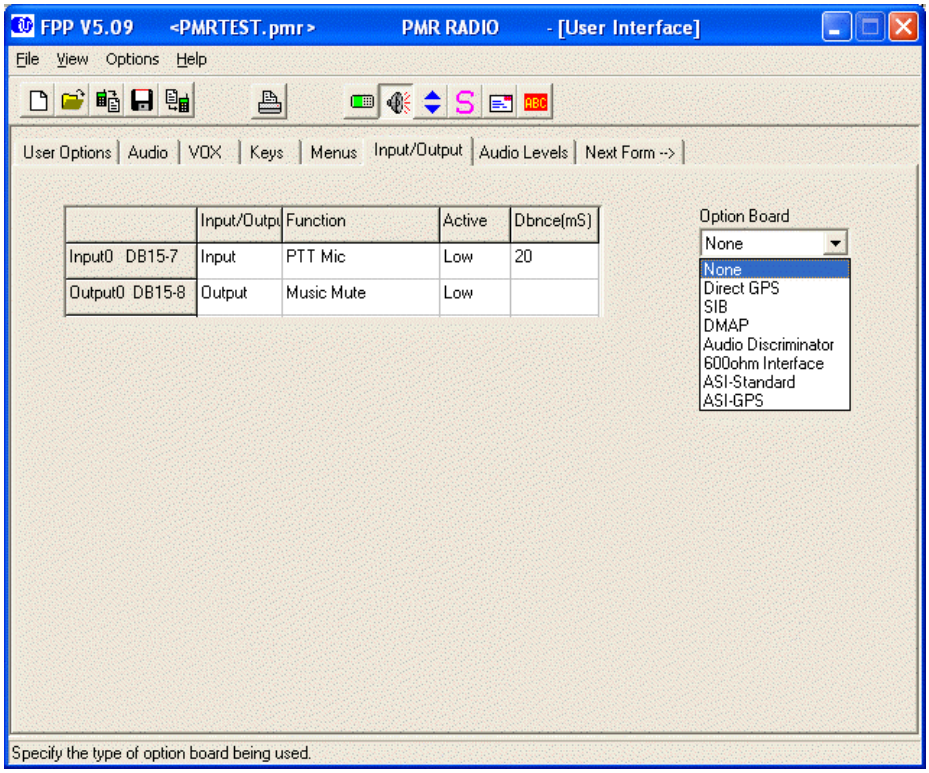


Figure 2.1 FPP Input/Output Menu Page

None defines a set of default pin-out functions when no option board is fitted. This is currently the same as for the “DMAP” selection.

Direct-GPS selects pin-out functions that support the GPS-Only Option Board. This principally reassigns the SPORT Port to accept serial data from the GPS engine.

SIB selects pin-out functions that support the Systems-Interface-Board (SIB) fitted with a Transcrypt Encryption module.
This sets the pin-outs up for interface to the additional CODEC and routes Transmit and Received audio via the CODEC for passing through the Encryption Module.

DMAP selects pin-out functions that support the Dual-Control Head, Dual-Transceiver, Serial/Parallel, and User-Applications General Purpose Interface (GPIF) Board.

Audio Discriminator (Not applicable for Rev 9) selects pin-out functions that support the Systems-Interface-Board (SIB) without a encryption module to provide a raw unsquelched discriminator output connection at the Radio DB15 connector (P2 pin 15).
This sets the pin-outs up for interface to the additional CODEC and routes Received Signal to the board (independent of User volume level).

600 Ohm Interface selects pin-out functions that support the 600 ohm interface board.
ASI Standard selects pin-out functions that support the ASI interface board. Along with other functionality, this board provides a raw unsquelched discriminator audio output connection.

ASI GPS selects pin-out functions that support the ASI interface board with GPS. Along with other functionality, this board provides a raw unsquelched discriminator audio output connection.

2.1.3 FPP Option-Board selection = "None"

None: This selects the default functions that support the standard radio.

The table below shows the 26-way Header pin functionality.

P1 Pin No	Other Connects	Name	IP/ OP	I/O Levels	Description
1	P2 pins 1,2,9,10	Ground	OP	0V	Ground.
2		Audio In / CCLK	OP	3.3V Logic 40mV RMS (60% MSD)	CCLK (Codec Clock, Direct DSP OP, 3.07/6.14MHz signal) Opt: Mic Audio to "Option Audio" via Option Board. R18=0R, (R246=0R prior Rev 9).
3		CLRC	OP	3.3V Logic	CLRC (Codec Left/Right Clock, Direct DSP Output).
4		PF4	IO	3.3V Logic, 100k pull-up to 3.3V.	Programmable Function.
5	P2 pins 4,6,11,12	13.8V Unsw	OP	13.8V and 0.1A.	Unswitched battery supply for Option Board.
6	P2 pin8	CONF2	OP	3.3V Logic	High Impedance inverted version of OP#0 on P2 pin 8. Direct DSP Output. Function as selected in FPP for OP#0.
7	P2 pins 4,6,11,12	13.8V Unsw	OP	13.8V and 0.1A.	Unswitched battery supply for Option Board.
8		SCLK2	OP	3.3V Logic	DSP Serial Port-1 Clock. Direct DSP Output, 7.68kHz.
9		IRESET	OP	3.3V Logic	Radio System RESET from Watchdog IC. Direct DSP Output. Low = RESET.
10		RFS	IP	3.3V Logic	DSP Serial Port-1 Receive-Frame-Sync. Direct DSP Input.
11		L3C	OP	3.3V Logic	Clock for Option-Board CODEC Synchronisation. Direct PLA Output.
12		TxD	OP	3.3V Logic	Serial comms with GPIF Board DSP, 768kB.
13		RxD	IP	3.3V Logic	Serial comms with GPIF Board DSP, 768kB.
14		TFS	OP	3.3V Logic	DSP Serial Port-1 Transmit-Frame-Sync. Direct DSP Output
15	S1 pin3 (via 1k res) P2 pin 15	Audio / PWR ON	IP OP	Approx 13V/0V Refer P2-15 for details	ON/OFF Line: Momentary Low to switch ON or OFF after release if held Low > 1.5sec. Low = <5V, High = >(Supply - 1.5V) or O/C. Internal 10k pull-up to +13.8V supply. Diode clamped to 0V and 18 Volts. Optional Audio connection to Audio O/P (P2 pin 15) via R67=NF, R68=0R, R94=0R. (R212=56R, R247=NF, R248=0R prior Rev 9).

16		L3D	OP	3.3V Logic	Data for Option-Board CODEC. Direct PLA Output.
17	S1 pin 5	13.8V Switched	OP	13.8V and 0.5A.	Poly fuse protected at 1Amp (at 25°C).
18		FC0	OP	3.3V Logic	Used to switch main GPIF Power On and Off. High = switch GPIF On.
19		L3M	OP	3.3V Logic	Configuration Mode waveform for CODEC. Direct PLA Output.
20	S8 pin 3, similar to P2 pin 7	Options PTT	IP	Low = <0.2V, High = > 1.5V or O/C. 100k input impedance with 10k pull-up to 5V.	Function determined by FPP IN#0 selection. Low = PTT.
21	P2 pin14	Option Audio	IP	40mV RMS (60% MSD)	External Tx Audio Input. Flat or Pre-emphasised, depending on IN#0 assignment (PTT Ext Data or PTT Ext). Sensitivity set by Audio Levels: Aux Input setting in FPP.
22	S1 pin 2	SIN	IP	3.3V Logic.	Controller Serial Input Data (19.2kBaud).
23	S1 pin 6, P2 pin 15 (prior Rev 9).	Audio Out (Refer Note 1 below).	OP	O/P from 50R source (O/C). 200mV RMS ---- O/P from 50R source (O/C). 535mV RMS ---- 535mV RMS ---- 40mV RMS ------ O/P from 50R source (O/C). 535mV RMS ---- 535mV RMS ----	**Discriminator Audio Output Signal. (Rev 9+)** Level set by: - Discriminator Level (Set typically to level 0). **Rx Audio Output Signal – Squelched. (Prior Rev 9)** Level set by: - User Volume (valid signal) set to 24 - Alert Offset (Beeps) set typically to 0. - Data-Volume (Level set typically to 15). **Optional Rx Audio Output Signal – Squelched.** **(Rev 9B):** R82=N.F. (Rev 9B), R871=0R (Rev 9B). **(Rev 9E+):** Programmable function. Level set by: - User Volume (valid signal) set to 24. - Alert Offset (Beeps) set typically to 0.
24		PF6	IO	3.3V Logic, 100k pull-up to 3.3V	Programmable Function
25	S1 pin 1	SOUT	OP	3.3V Logic	Controller Serial Output Data (19.2kBaud)
26	Same as pin 1	Ground	IO	0V	Ground

Table 1: Pin-out Assignments for Standard Radio Functionality

Note 1. Some builds of Rev 9B have functionality and component differences to current values.

ie. prior S/N:- 3R**X05460DL9, 5R**X054853VH (T934): R856=47k and R857=47k.
prior S/N:- 3R**X05491JBW ,5R**X054853VH (T939): R82=NF and R871=1k.
S/N:- 3R**X05460DL9, 5R**X054853VH to TBA. (T934/T972): R856=33k and R857=68k.
S/N:- 5R**X054853VH to TBA, (T939/T972): R82=1k and R871=N.F.
From S/N:- TBA to Rev 9E, (T972): R856=27k, R82=0R, R87=560R, R97=N.F. and link R92/R94 to C855/R871.
Rev 9E+: Refer to schematic diagrams if non-standard modifications are required. In addition, an FPP programmable analogue gate has been added to improve audio switching flexibility.

2.1.4 FPP Option-Board selection = "Direct-GPS"

This selects pin-out functions that support the GPS-Only Option Board.
This principally reassigns the SPORT Port to accept serial data (at 4800 baud) from the GPS engine.
Functions that have changed from those shown in Table-1 are:

P1 Pin No	Other Connects	Name	IP/ OP	I/O Characteristics	Description
13		RxD	IP	3.3V Logic	Receives 4800 baud data stream in NMEA0183 format (from GPS Engine)

2.1.5 FPP Option-Board selection = "SIB"

SIB selects pin-out functions that support the Systems Interface Board (SIB) fitted with a Transcrypt Encryption module.
This sets the pin-outs up for interface to the additional CODEC and routes Transmit and Received audio input/output of the CODEC for passing through the Encryption Module.
Functions that have changed from those shown in Table 1 are:

P1 Pin No	Other Connects	Name	IP/ OP	I/O Characteristics	Description
4		PF4	OP	3.3V Logic	Switches Scrambler to "Transmit" when User PTT pressed Hi = Radio Receiving, Lo = Radio Transmitting.
6		CONF2	OP	3.3V Logic	Toggles Hi/Low with "Scrambler-4" Output Function (Refer AN: A9k-301)
23	S1 pin 6, P2 pin 15 (prior Rev 9)	Audio Out	IP	I/P from 560R source (O/C).	Discriminator Audio Output Signal from SIB to P2-15. C855=N.F. (Rev 8, 9E+), C857=N.F. (Rev 9B), R82=0R (Rev 9+).
24		PF6	OP	3.3V Logic	Toggles Hi/Low with "Scrambler-2" Button Function. (Refer AN: A9k-301)

2.1.6 FPP Option-Board selection = "DMAP"

DMAP: This selects functions that support the Dual-Control Head, Dual-Transceiver, Serial/Parallel, and User-Applications (DMAP) Boards.

Functions and levels are identical to those shown in Table 1.

2.1.7 FPP Option-Board selection = "Audio Discriminator"

Audio Discriminator (Prior Rev 9) selects pin-out functions that support the Systems Interface Board (SIB) (without an encryption module) to provide a raw Discriminator Output connection at the Transceiver DB15 connector (pin 15).
This sets the pin-outs up for interface to the additional CODEC and routes Received Signal to the board (independent of User volume level).

Note 1. H/S Audio will be unmuted when this function is active.

Note 2. This function is not relevant for Rev 9+. Discriminator Audio is available directly with optional jumpering on Rev 9+ and is independent to H/S Audio.

Functions that have changed from those shown in Table 1 are:

P1 Pin No	Other Connects	Name	IP/ OP	I/O Characteristics	Description
23	S1 pin 6, P2 pin 15	Audio Out	IP	I/P from 560R source (O/C).	**Discriminator Audio Output Signal from SIB to P2-15.** C855=N.F., C857=N.F.

2.1.8 FPP Option-Board selection = "600ohm Interface"

600ohm Interface selects pin-out functions that support the 600ohm Interface Board.

Functions and levels are identical to those shown in Table 1.

2.1.9 FPP Option-Board selection = "ASI Standard"

ASI Standard selects pin-out functions that support the ASI Standard Interface Board.

Functions that have changed from those shown in Table 1 are:

P1 Pin No	Other Connects	Name	IP/ OP	I/O Characteristics	Description
12		TxD	OP OP	3.3V Logic 200mV RMS O/C from 600R source.	PWM audio O/P (Prior Rev 9). SIB RJ8 connector.
23	S1 pin 6, P2 pin 15 (prior Rev 9).	Audio Out	OP	O/P from 50R source (O/C). 200mV RMS ----	**Discriminator Audio Output Signal. (Rev 9+)** Level set by: - Discriminator Level (Set typically to level 0).

2.1.10 FPP Option-Board selection = "ASI GPS"

ASI GPS selects pin-out functions that support the ASI GPS Interface Board.

Functions that have changed from those shown in Table 1 are:

P1 Pin No	Other Connects	Name	IP/ OP	I/O Characteristics	Description
12		TxD	OP	3.3V Logic	PWM audio O/P (Prior Rev 9)
23	S1 pin 6, P2 pin 15 (prior Rev 9).	Audio Out	OP	O/P from 50R source (O/C). 200mV RMS ----	**Discriminator Audio Output Signal. (Rev 9+)** Level set by: - Discriminator Level (Set typically to level 0).

2.2 15 Way DB15 Connector (Connector P2)

A male DB15 connector is provided for interfacing internal radio functions to external devices.

P2 Pin No	Other Connects	Name	IP/ OP	I/O Levels	Description
1		GROUND	IP	0V and 2 amps	Battery input.
2		GROUND	IP	0V and 2 amps	Battery input.
3		IGN	IP	Approx 13.8V/0V	Ignition sense input. Switch high to enable.
4		BATTERY IN	IP	Approx 13.8V and 2 amps.	Battery input.
5		BATTERY IN	IP	Approx 13.8V and 2 amps.	Battery input.
6		SPEAKER (+)	OP	4V RMS at 4W output.	Speaker output.
7		MF21 (IN#0)	IO	3V3 or 5V logic	General purpose I/O or Ext. PTT input.
8		MF23 (OUT#0)	OP	O/C or 190mA sink.	Relay driver, etc. from nominal 13.8V battery source. Note. 80mA max prior Rev 9.
8	S5 pin 11	MF23 (OUT#0)	IO	3V3 logic	General purpose I/O. R50=1k, R51=1k, R61=1k.
9		GROUND	IP	0V and 2 amps	Battery input.
10		GROUND	IP	0V and 2 amps	Battery input.
11		BATTERY IN	IP	Approx 13.8V and 2 amps.	Battery input.
12		BATTERY IN	IP	Approx 13.8V and 2 amps.	Battery input.
13		SPEAKER (-)	OP	Speaker return	Differential O/P for 10W setting. R859=0R, Speaker=8R.
14	P1 pin 21	MF19 (AUDIO I/P)	IP	40mV RMS (60% MSD)	External Tx Audio Input. Flat or Pre-emphasised, depending on IN#0 assignment (PTT Ext Data or PTT Ext). Sensitivity set by Audio Levels: Aux Input setting in FPP. R21=NF (R89=NF prior Rev 9).
15		Audio Out (Refer Note 1).	OP	O/P from 600R source (O/C). 535mV RMS ---- 535mV RMS ---- 40mV RMS ------ O/P from 600R source (O/C). 535mV RMS ---- 535mV RMS ---- O/P from 600R source (O/C). 200mV RMS ----	**Rx Audio Output Signal – Squelched. (Prior Rev 9)** Level set by: - User Volume (valid signal) set to 24 - Alert Offset (Beeps) set typically to 0. - Data-Volume (Level set typically to 15). **Rx Audio Output Signal – Squelched. (Rev 9+)** R82=0R, C857=NF. (Rev 9B). Level set by: - User Volume (valid signal) set to 24. - Alert Offset (Beeps) set typically to 0. **Optional Discriminator Audio Output Signal.** **Rev 9B:** R82=N.F. C857=10uF. **Rev 9E+:** Programmable function. Level set by: - Discriminator Level (Set typically to level 0).

2.3 19 Way Hirose Connectors (Connectors S5, P6, S8 on Rev 9+ only)

Radios using Revision 9 and later PCBs also have three 19 way Hirose connectors provided.

Two of these duplicate the above 26 way connector functionality as well as providing additional functionality and are the means of interfacing the radio PCB with several internally installed Option PCBs.
Some of these Option PCBs can also have the ability to provide additional external interface functions.

The other 19 way Hirose connector P6 provides a means of directly programming the Flash Memory as an alternative to the Serial Interface and is required for programming new unprogrammed or corrupted Flash Memory.

S5 Pin No	Other Connects	Name	IP/ OP	I/O Characteristics	Description
1		0VA	IO	0V	Common ground
2		ANALOG_ IN	IP	0V to 2.5V.	Radio can be programmed to detect analog input levels. R52=1k, R53=1k.
3		MF10	IO	3.3V Logic	General purpose I/O. R40=1k, R41=1k.
4		MF11	IO	3.3V Logic	General purpose I/O. R38=1k, R39=1k, R82=NF, R871=NF, R872=NF (Rev 9E+).
4	P1 pin 23	AUDIO_O UT1 (Refer Note 1).	OP	O/P from 50R source (O/C). 200mV RMS ---- O/P from 50R source (O/C). 535mV RMS ---- 535mV RMS ----	**Discriminator Audio Output Signal. (Rev 9+)** R38=0R. Level set by: - Discriminator Level (Set typically to level 0). **Optional Rx Audio Output Signal – Squelched. (Rev 9+)** R82=N.F. (Rev 9B), R872=N.F. (Rev 9E+), R871=0R (Rev 9+). Level set by: - User Volume (valid signal) set to 24. - Alert Offset (Beeps) set typically to 0.
5		MF12	IO	3.3V Logic	General purpose I/O.
6		MF13	IO	3.3V Logic	General purpose I/O.
7		MF14	IO	3.3V Logic	General purpose I/O.
8		MF15	IO	3.3V Logic	General purpose I/O.
9		MF16	IO	3.3V Logic	General purpose I/O.
10		MF17	IO	3.3V Logic	General purpose I/O. R42=1k, R43=1k, R30=NF.
10	P1 pin 21	OPTION AUDIO	IO	40mV RMS (60% MSD)	External Tx Audio Input. Flat or Pre-emphasised, depending on IN#0 assignment (PTT Ext Data or PTT Ext). Sensitivity set by Audio Levels: Aux Input setting in FPP. R42=1k. Refer to schematics for additional connection details.
11		MF23	IO	3.3V Logic	General purpose I/O. R50=1k, R51=1k.
11	P2 pin 8	MF23A	IO	3.3V Logic	General purpose I/O. R50=1k, R51=1k, R61=1k.
12		MF18	IO	3.3V Logic	General purpose I/O.
13		+5V	OP	5 volts at 50mA max.	Option board supply.
14		MF19	IO	3.3V Logic	General purpose I/O. R44=1k, R45=1k.
14	P2 pin14	MF19	IO	3.3V Logic	General purpose I/O. R44=1k, R45=1k, R56=1k.
15		MF20	IO	3.3V Logic	General purpose I/O. R46=1k, R47=1k.

15	S1 pin 3	On/Off	IO	3.3V Logic	General purpose I/O. R46=NF, R47=1k, R64=1k.
15	P2 pin 15	AUDIO O/P	OP	AUDIO O/P	Rx Audio Output Signal. R46=1k, R47=1k, R94=1k. Refer to P1 pin 23 and schematics for more information
16		MF21	IO	3.3V Logic	General purpose I/O. R48=1k, R49=1k.
17		0VA	IO	0V	Common ground
18		MF9	IO	3.3V Logic	General purpose I/O.
19		13V8_UNSW_F	OP	13.8V at 100mA max.	Unswitched battery supply via radio.

P6 Pin No	Other Connects	Name	IP/ OP	I/O Characteristics	Description
1		3V3	OP	3.3 volts at 20mA max.	Flash Programmer supply.
2		TMS	IO	3.3V Logic	Flash Programmer function.
3		TRST	IO	3.3V Logic	Flash Programmer function.
4		0VA	IO	3.3V Logic	Flash Programmer function.
5		TCK	IO	3.3V Logic	Flash Programmer function.
6	S8 pin 13	/RESET	OP	3.3V Logic	System reset when low.
7		ERES	IO	3.3V Logic	Flash Programmer function.
8		EE	IO	3.3V Logic	Flash Programmer function.
9		EMS	IO	3.3V Logic	Flash Programmer function.
10		ELOUT	IO	3.3V Logic	Flash Programmer function.
11		ECLK	IO	3.3V Logic	Flash Programmer function.
12		TDO	IO	3.3V Logic	Flash Programmer function.
13		ELIN	IO	3.3V Logic	Flash Programmer function.
14		EBR	IO	3.3V Logic	Flash Programmer function.
15		EINT	IO	3.3V Logic	Flash Programmer function.
16		EBG	IO	3.3V Logic	Flash Programmer function.
17		/BR	IO	3.3V Logic	Flash Programmer function.
18		TDI	IO	3.3V Logic	Flash Programmer function.
19		/BG	IO	3.3V Logic	Flash Programmer function.

S8 Pin No	Other Connects	Name	IP/ OP	I/O Characteristics	Description
1		BAT_SW	OP	13.8V at 100mA max.	Switched battery supply for option board supply. (SW_BAT on P25 option board, MAB2)
2		RX_DATA 1	IP	3.3V Logic.	Controller Serial Input Data (19.2kBaud). (RXD1 on P25 option board, MAB2)
3	P1 pin 20, similar to P2 pin 7.	PTT_IN2	IO	Low = <0.2V, High = > 1.5V or O/C 100k input impedance with 10k pull-up to 5V.	Function determined by FPP IN#0 selection. Low = PTT. (PTT on P25 option board).
4		MF5	IO	3.3V Logic.	General purpose I/O. (TXD0 Serial Input Data to Controller. (768/1536kBaud) on P25 option board). 60kb/S on MAB2. TXD0 on MAB2
5		MF6	IO	3.3V Logic.	(MCK1 on P25 option board, MAB2, 30.72MHz).
6		TX_DATA 1	OP	3.3V Logic.	Controller Serial Output Data (19.2kBaud). (RXD1 on P25 option board)

7		MF25	IO	3.3V Logic.	General purpose I/O.
8		0VA	IO	0V	Common ground
9		L3M_B	IO	3.3V Logic.	General purpose I/O.
10		0VA	IO	0V	Common ground
11		MF2	IO	3.3V Logic.	General purpose I/O. R34=NF, R35=0R. Not connected for MAB2
11		3V3	OP	3.1 volts at 20mA max.	Option board supply. R34=10R, R35=NF.
12		RXD	IP	3.3V Logic	SPORT0 Serial Input Data (768/1536kBaud).
13		/RESET	OP	3.3V Logic	System reset when low.
14		TXD	OP	3.3V Logic	SPORT0 Serial Output Data (768/1536kBaud).
15		MF24	IO	3.3V Logic	General purpose I/O.
16		MF3	IO	3.3V Logic	General purpose I/O. (SCLK0 on P25 option board, MAB2).
17		MF4	IO	3.3V Logic	General purpose I/O. (nReset on P25 option board, MAB2).
18		MF7	IO	3.3V Logic	General purpose I/O. (RXD0 Serial Output Data from Controller. (60kb/s) on P25 option board, MAB2).
19		MF8	IO	3.3V Logic	General purpose I/O. R36=0R, R37=NF. (Not connected, MAB2)
19		+5V	OP	4.8 volts at 20mA max.	Option Board Supply. R36=NF, R37=10R.

2.4 8 Way RJ8 Connector

An RJ8 socket is provided for interfacing internal radio functions to control devices such as a Microphone, Control Head or Controller Handset.

S1 Pin No	Other Connects	Name	IP/ OP	I/O Characteristics	Description
1	P1 pin 25	Tx Data	OP	3.3V Logic	Controller Serial Output Data (19.2kBaud).
2	P1 pin 22	Rx Data	IP	3.3V Logic.	Controller Serial Input Data (19.2kBaud).
3	P1 pin 15 (via 1k res)	On/Off	IP	Approx 13V/0V	ON/OFF Line: Momentary Low to switch ON or OFF after release if held Low > 1.5sec.
4		0VA	IP	0V	Ground return for mic audio.
5	P1 pin 17	13V8_SW	OP	13.8V at 500mA	Switched battery supply via radio.
6		H/S Audio	OP	O/P from 50R source (O/C). 500mV RMS ---- 500mV RMS ---- 40mV RMS ------ O/P from 50R source (O/C). 500mV RMS ---- 500mV RMS ---- 40mV RMS ------	**Rx Audio Output Signal – Squelched. (Prior Rev 9)** Level set by: - User-Volume (valid signal) set to 24 - Alert Offset (Beeps) set typically to 0. - Data-Volume (Level set typically to 15). **Rx Audio Output Signal – Squelched. (Rev 9+)** Level set by: - User-Volume (valid signal) set to 24. - Alert Offset (Beeps) set typically to 0. - Data-Volume (Level set typically to 15).
7		0VA	OP	0V	Ground return for functions other than Mic Audio.
8		Mic Audio	IP	40mV RMS (60% MSD)	Input impedance: 1k2 approx.

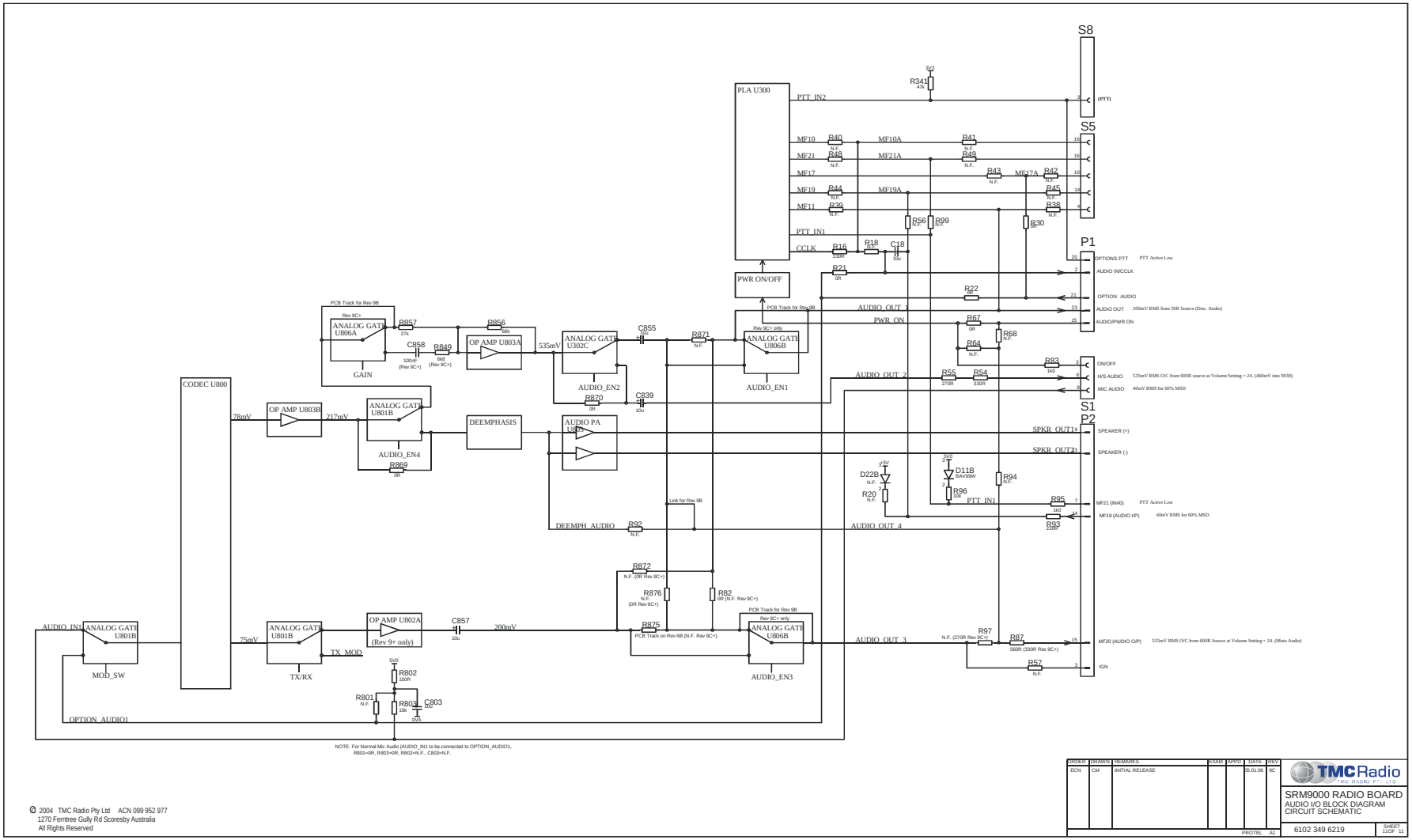
2.5 2 Way Hirose Connectors (Connectors P3 and P4 on Rev 9+ only)

Radios using Revision 9B and later PCBs have provision for adding two single function Hirose connectors that are intended for external 14.4MHz reference oscillator input and an internal connection for battery supply.

If required, the Hirose part number is DF3-2P-2H. When fitted together with relevant jumpers they default to the functions as detailed below.

Alternatively, they can be hard wired to other alternative internal functions if required by omitting the jumpers.

Pin No	Other Connects	Name	IP/ OP	I/O Characteristics	Description
P3-1	P2 pins 4,6,11,12	13V8_UNSW	OP	13.8V at 200mA max.	Unswitched battery supply via radio. R27=0R
P3-2	P2 pins 1,2,9,10	0VA	OP	Ground	Ground return for the above. R26=0R
P4-1		EXT_REF	IP	14.4MHz	High stability reference. R29=0R, U700=NF
P4-2		0VA	IP	Ground	Ground return for the above. R28=0R



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PROTEL A1

Figure 1 Audio Routing Block diagram